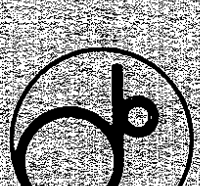

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CAMAC STANDARD MODULES FOR HIGH ENERGY PHYSICS EXPERIMENTS AT KEK

by

Susumu INABA, Eiji INOUE, Mitsuo IKEDA, Masahiro IKENO,
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NATIONAL LABORATORY FOR
HIGH ENERGY PHYSICS

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Abstract

The data acquisition system of the high energy experiment demands various kinds of electronics. The standardized units of the modular configuration are designed and built under the specifications of NIM and CAMAC standards. We have already published the specifications of the NIM modules preferentially used at KEK (KEK-EXP. FACILITIES-77-2) in 1977. This paper is associated with the NIM modules , and describes the specifications and schematics of the CAMAC modules which include standard modules designed by the Electronics Group in the Physics Department.

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APPENDIX

1. Introduction

The CAMAC modular system has been adopted as a standard data acquisition system in KEK from 1970. The CAMAC system is the general purpose modular electronics instrumentation standard for data handling. In all areas where process control, data logging or data processing are requirements, the CAMAC can provide rapid bi-directional communication between systems and computers. All instruments from this modular data transfer system are mechanically and electrically compatible. They communicate via the dataway in a standard fashion, enabling a wide variety of transducers and other devices to be readily connected to an extensive range of digital controllers or computers. The CAMAC specification conforms to standards set up by ESONE Committee (European Standards on Nuclear Electronics), which consists of representatives from major research organizations of thirteen European nations. The United States NIM Committee has endorsed CAMAC so the system is accepted as "International Standard". Recently, the CAMAC standards have world-wide acceptance not only in the field of nuclear electronics, but also in various application. The CAMAC involves every aspects of the data acquisition and control system, such as modular functional units system, serial data transmission, distributed intelligence with micro-computers and soft-ware. Those CAMAC standard papers have been published by ECA (European CAMAC Association) and US DOE (Department of Energy) as listed in Table 1.

This paper is a collection of individual manuals of standardized CAMAC modules at KEK. It would facilitate to use CAMAC system in the high energy physics experiment. Useful tables and figures of the CAMAC standards are compiled in the Appendix.

2. CAMAC Modules and Related Items

The following papers are short form manuals of CAMAC modules and related items including commercial ones. These are provided for the high energy physics experiments by the Electronics Group in the Physics Department at KEK. All modules and related items are numbered as follows to meet the convenience of the stock management.

CX(1)X(2)-Y(1)Y(2)-ZZZ
NX(1)X(2)-Y(1)Y(2)-ZZZ

C : Means CAMAC modules.
N : Means NIM modules.
X(1)X(2) : Functional group code number of modules.
Y(1) : Specific functional code number of modules.
Y(2) : Means a kind of module.
(For example, Y(2)=0 means commercial modules.)
ZZZ : Serial number of modules.

Up to now, the number of modules amounts to about 4000 including both NIM and CAMAC modules. These are always under control by the Electronics Group, and are distributed to many users and maintained.

Table 1

SPECIFICATIONS AND SUPPLEMENTARY INFORMATION

CAMAC Specifications

	Description	Publications by the Commission of the European Communities and the ESONE Committee	Corresponding documents of publications by other bodies			
			US Department of Energy and US NIM Committee	Published by IEEE,ANSI	Published by IEC	Published by CMEA
1	A Modular Instrumentation System for Data-Handling	EUR 4100e (1972)(English) EUR 4100f (1972)(French) EUR 4100i (1972)(Italian)	TID-25875*	IEEE Std.583++ (1975)	IEC Publ.482 IEC Publ.516	4572-74 and 4573-74
2	Block Transfers in CAMAC Systems	EUR 4100 supp.	TID-26616*	IEEE Std.683 (1976)	45(CO)129	
3	Organisation of Multi-Crate Systems (Parallel Branch Highway)	EUR 4600e (English) EUR 4600f (French) EUR 4600i (Italian)	TID-25876*	IEEE Std.596 (1976)	IEC Publ.552	in preparation
4	Specifications of Amplitude Analogue Signals within a 50 Ω System	EUR 5100e (1974)	TID-26614			in preparation
5	Supplementary Information on CAMAC Instrumentation System	Supplement to CAMAC Bulletin Issue 6	TID-25877	Part of IEEE Std.583 and 596		
6	CAMAC Serial Highway System and Serial Crate Controller Type L2	EUR 6100e		IEEE Std.595++ (1976)	IEC Publ.640	in preparation
7	The Definition of IML. A Language for Use in CAMAC Systems	ESONE/IML/01	TID-26615			
8	Real-Time BASIC for CAMAC	ESONE/RTB/02 (amended version of RTB/01)	TID-26619	IEEE Std.726** (1979)		
9	Recommendations for CAMAC Serial Highway Drivers and LAM Graders for the SCC-L2	ESONE/SD/02	DOE/EV-0006			
10	Multiple Controller in a CAMAC Crate	EUR 6500e	DOE/EV-0007	IEEE Std.675++ (1979)	45(CO)130	
11	Subroutine for CAMAC	ESONE/SR/01	DOE/EV-0016	IEEE Std.758		
12	Definitions of CAMAC Terms used in ESONE Specifications	ESONE/GEN/01	DOE/EV... in preparation			
13	Revision of ESONE CAMAC Documents	ESONE/DOC/01	DOE/EV-0009+	IEEE Std.583A+ (in preparation)		

Availability of Documents

Office for Official Publications of the European Communities P.O.Box 1003 Luxembourg	EUR-Documents
ESONE/ECA Secretariat c/o Commission des Communautés Européennes, CCR-BCMN B-2440 Geel	ESONE-Documents EUR-Documents (to a limited extent for ESONE/ECA members)
National Bureau of Standards Washington D.C. 20234, USA Attn.: L. Costrell	DOE and TID-Documents
IEEE Service Center 445 Hoes Lane Piscataway New Jersey 08854, USA	IEEE-Documents
International Electrotechnical Commission, Secretariat 1 Rue de Varembé CH-1211 Genève 20	IEC-Documents
CMEA Secretary Prospekt Kalinina 56 Moskva, USSR	CMEA-Documents

*) no more available and superseded by IEEE Std. Publications
**) not fully identical with ESONE/RTB/02 and TID-26619
+) revision of corresponding documents issued in the US
++) also American Standard-ANSI with the same designation as the respective IEEE Standard

TYPE MODULENM.SR
MODULENM.SR

DATE MAY 26,1980
THE STOCK LIST OF KEK STANDARD MODULES FOR COUNTER EXPERIMENTS

(1) NIM MODULE AND RELATED ITEMS

N-00	NIM BLANK MODULE CASE
N-01	NIM BIN AND NIM FRAME
N-02	NIM POWER SUPPLY
N-03	NIM COOLING FAN
N-04	FIXED AND VARIABLE ATTENUATOR
N-05	FIXED AND VARIABLE DELAY
N-06	FAST,SLOW AND ZERO CROSSING DISCRIMINATOR
N-07	COINCIDENCE AND MALTIPLICITY LOGIC
N-08	FAST AND SLOW LINEAR AMPLIFIER
N-09	LINEAR AND LOGIC FAN IN/ FAN OUT
N-10	LINEAR ADDER AND LINEAR GATE
N-11	GATE GENERATOR AND GATE DRIVER
N-12	SCALER AND PRESET CONTROLLER
N-13	PULSE GENERATOR
N-14	DIGITAL VOLTMETER
N-15	LOGIC LEVEL ADAPTER
N-16	A-D,T-D CONVERTER AND VOLTAGE INTEGRATOR
N-17	INTERRUPT CONTROLLER
N-18	PRINTER CONTROLLER

(2) CAMAC MODULE AND RELATED ITEMS

C-00	CAMAC BLANK MODULE CASE
C-01	CAMAC CRATE
C-02	CAMAC POWER SUPPLY
C-03	MODULE EXTENDER
C-04	CRATE CONTROLLER
C-05	BRANCH DRIVER
C-06	BRANCH TERMINATOR AND BRANCH TRANSCEIVER
C-07	POWER INDICATOR
C-08	IN/OUT, INTERRUPT, COINCIDENCE, AND SWITCH REGISTER
C-09	LAM GRADER
C-10	SCALER AND PRESET COUNTER
C-11	A-D AND T-D CONVERTER
C-12	PULSE GENERATOR
C-13	NIM MODULE AND TTY/CRT INTERFACE
C-14	FAN IN AND FAN OUT
C-15	MEMORY BUFFER
C-16	PROGRAMMABLE ATTENUATOR AND DELAY

(3) ACCESSORY EQUIPMENT FOR NIM AND CAMAC MODULE

A-01	BNC AND LEMO SIGNAL CABLE
A-02	BNC AND LEMO 50-OHM TERMINATOR
A-03	DATAWAY AND POWER SUPPLY CABLE

(1) NIM MODULE

	NUMBERS
N-00-11 NIM BLANK MODULE CASE KEK TYPE-1	
N-01-10 NIM BIN	0003
N-01-11 NIM BIN KEK TYPE-1 (WITH POWER CABLE)	0108
N-01-21 NIM BIN KEK TYPE-2 (WITH DATA WAY AND POWER CABLE)	0049
N-01-30 NIM BIN POWERED (12V-2A,24V-1A)	0003
N-01-41 NIM BIN FRAME KEK TYPE-1	0070
N-02-11 NIM POWER SUPPLY KEK TYPE-1 (6V-10A,12V-4A,24V-2A)	0023
N-02-11 NIM POWER SUPPLY KEK TYPE-2 (6V-28A,12V-6A,24V-4A)	0041
N-02-21 6V POWER SUPPLY MODULE (6V-2A) KEK TYPE-1	0002
N-02-30 HIGH VOLTAGE POWER SUPPLY (ORTEC 456)	0002
N-03-10 NIM COOLING FAN	0002
N-03-11 NIM COOLING FAN KEK TYPE-1	0130
N-04-11 DUAL VARIABLE ATTENUATOR (0-31DB) KEK TYPE-1	0450
N-05-11 DUAL VARIABLE DELAY (0-31NS) KEK TYPE-1	0500
N-05-21 FIXED DELAY (100NS) KEK TYPE-1	0100
N-05-22 DUAL FIXED DELAY (100NS) KEK TYPE-1	0070
N-05-23 FIXED DELAY (200NS) KEK TYPE-2	0050
N-05-31 16-CH FIXED LOGIC DELAY (105NS) KEK TYPE-1	0025
N-06-10 DUAL DISCRIMINATOR (EGG T105/NL)	0006
N-06-10 OCTAL DISCRIMINATOR (LECROY 620L)	0001
N-06-10 QUAD DISCRIMINATOR (LECROY 621L)	0001
N-06-10 QUAD DISCRIMINATOR (EGG T120/N)	0001
N-06-11 DUAL DISCRIMINATOR KEK TYPE-1	0001
N-06-20 OCTAL UPDATING DISCRIMINATOR (LECROY 623)	0059
N-06-20 OCTAL UPDATING DISCRIMINATOR (ORTEC 928)	0008
N-06-20 QUAD UPDATING DISCRIMINATOR (EGG T122/NL)	0006
N-06-21 QUAD NON-UPDATING DISCRIMINATOR KEK TYPE-1	0010
N-06-22 QUAD NON-UPDATING DISCRIMINATOR KEK TYPE-2	0120
N-06-22 QUAD UPDATING DISCRIMINATOR KEK TYPE-1	0040
N-06-30 QUAD ZERO CROSSING DISCRIMINATOR (EGG T140/NL)	0013
N-06-30 QUAD CONSTANT FRACTION DISCRIMINATOR (EGG 934)	0002
N-06-30 QUINT RISETIME COMPENSATED DISCRIMINATOR (LECROY 825)	0001
N-06-31 QUAD CONSTANT FRACTION DISCRIMINATOR KEK TYPE-1	0120
N-06-40 DIFFERENTIAL DISCRIMINATOR (EGG TD101/NL)	0002
N-06-50 MEAN TIMER (SEN FE257)	0002
N-06-50 OCTAL MEAN TIMER (LECROY 624)	0010
N-06-60 TIMING SINGLE CHANNEL ANALYZER (ORTEC 551)	0002

	NUMBERS
N-07-10 QUAD 2-FOLD LOGIC UNIT (LECROY 622)	0011
N-07-10 QUAD 2-FOLD LOGIC UNIT (LECROY 322A)	0002
N-07-20 4-FOLD 1-VETO COINCIDENCE (EGG C144/N)	0001
N-07-21 DUAL 4-FOLD 1-VETO COINCIDENCE KEK TYPE-1	0105
N-07-22 TRIPLE 4-FOLD 1-VETO COINCIDENCE KEK TYPE-1	0020
N-07-30 DUAL 4-FOLD MAJORITY LOGIC UNIT (LECROY 365AL)	0011
N-07-40 32-INPUT MULTIPLICITY LOGIC UNIT (LECROY 380)	0004
N-07-40 32-INPUT MULTIPLICITY LOGIC UNIT (LECROY 380A)	0017
N-07-42 12-CH MATRIX LOGIC UNIT KEK TYPE-1	0002
N-07-43 8-INPUT PRIORITY LOGIC UNIT KEK TYPE-1	0005
N-07-51 8-FOLD 1-VETO COINCIDENCE KEK TYPE-1	0028
N-07-61 OCTAL STROBED COINCIDENCE KEK TYPE-1	0070
N-08-10 QUAD AMPLIFIER (EGG AN201/NL)	0004
N-08-10 12-CH PHOTO-MULTIPLIER AMPLIFIER (GAIN FIXED X10)(LECROY 612)	0017
N-08-10 6-CH PHOTO-MULTIPLIER AMPLIFIER (GAIN VARIABLE X40)(LECROY 612M)	0007
N-08-11 OCTAL PULSE AMPLIFIER (GAIN FIXED X8) KEK TYPE-1	0050
N-08-20 PICK-UP AMPLIFIER (BORER 511)	0002
N-08-20 DUAL BIPOLAR LINEAR AMPLIFIER (LECROY 234)	0001
N-08-30 SHAPING AMPLIFIER (SEN FE280)	0004
N-08-30 DUAL SUM AND INVERT AMPLIFIER (ORTEC 433A)	0001
N-08-30 GATED BIASED AMPLIFIER (ORTEC 444)	0001
N-08-40 SPECTROSCOPY AMPLIFIER (ORTEC 472)	0006
N-09-10 QUAD LOGIC FAN-IN/FAN-OUT (LECROY 429)	0012
N-09-11 QUAD 4-INPUT OR LOGIC UNIT KEK TYPE-1	0030
N-09-12 QUAD LOGIC FAN-IN/FAN-OUT KEK TYPE-2	0020
N-09-20 DUAL FANOUT (SEN FE271)	0002
N-09-21 DUAL FANOUT KEK TYPE-1	0025
N-09-22 DUAL FANOUT KEK TYPE-2	0090
N-09-23 32-OUTPUT FANOUT KEK TYPE-3	0030
N-09-24 DUAL LOGIC FAN-IN/FAN-OUT KEK TYPE-1	0030
N-09-25 OCTAL FANOUT KEK TYPE-1	0040
N-09-26 QUAD FANOUT KEK TYPE-1	0020
N-10-10 DUAL BIPOLAR LINEAR FANIN (LECROY 127DL)	0001
N-10-10 DUAL BIPOLAR LINEAR FANIN (LECROY 127FL)	0002
N-10-10 QUAD LINEAR FANIN/FANOUT (LECROY 428A)	0005
N-10-10 QUAD LINEAR FANIN/FANOUT (LECROY 428F)	0027
N-10-10 DUAL LINEAR MIXER (EGG AN308/NL)	0045
N-10-11 DUAL LINEAR MIXER KEK TYPE-1	0003
N-10-12 OCTAL SIGNAL DIVIDER KEK TYPE-1	0100
N-10-20 LINEAR GATE (SEN FE281)	0003
N-10-20 LINEAR GATE (EGG LG101/N)	0008
N-10-20 LINEAR GATE AND STRETCHER (EGG LG105/NL)	0005
N-10-20 LINEAR GATE AND STRETCHER (ORTEC 442)	0001

		NUMBERS
N-11-10	GATE AND DELAY GENERATOR (ORTEC 416A)	0004
N-11-10	DUAL GATE GENERATOR (LECROY 222)	0022
N-11-11	DUAL GATE GENERATOR KEK TYPE-1	0025
N-11-20	FAST TRIGGER UNIT (EGG T200/N)	0002
N-11-21	OCTAL FAST TRIGGER UNIT KEK TYPE-1	0010
N-11-31	SCALER GATE DRIVER KEK TYPE-1	0025
N-11-41	BEAM SPILL GATE GENERATOR KEK TYPE-1	0006
N-12-10	200MHZ PRE SCALER (1-DIGIT)(EGG S110/N)	0001
N-12-11	100MHZ VISUAL SCALER (6-DIGIT) KEK TYPE-1	0014
N-12-21	60MHZ VISUAL SCALER (6-DIGIT) KEK TYPE-1	0057
N-12-22	80MHZ VISUAL SCALER (6-DIGIT) KEK TYPE-2	0175
N-12-31	PRESET SCALER CONTROLLER (6-DIGIT) KEK TYPE-1	0028
N-12-41	SCALER AUTOMATIC TESTER KEK TYPE-1	0002
N-12-51	PRESET SCALER (3-DIGIT) KEK TYPE-1	0020
N-12-52	DUAL PRESET SCALER (3-DIGIT) KEK TYPE-1	0010
N-12-61	HEX 80MHZ VISUAL PRE SCALER (1-DIGIT) KEK TYPE-1	0020
N-13-10	NORMALIZING PULSE GENERATOR (TOYO BM910)	0002
N-13-10	125MHZ PULSE GENERATOR (BNC 8020)	0004
N-13-10	50MHZ PULSE GENERATOR (BNC 8010)	0008
N-13-11	10MHZ PULSE GENERATOR KEK TYPE-1	0025
N-13-20	RANDOM PULSE GENERATOR (BNC DB-2)	0002
N-14-11	DIGITAL VOLTMETER (3.5-DIGIT) KEK TYPE-1	0002
N-15-11	QUAD NIM TO CAMAC LEVEL ADAPTER KEK TYPE-1	0020
N-15-21	TRIPLE TTL TO NIM LEVEL ADAPTER KEK TYPE-1	0010
N-15-30	QUAD LOGIC LEVEL ADAPTER (EGG LI380/ML)	0010
N-15-31	QUAD LOGIC LEVEL ADAPTER KEK TYPE-1	0030
N-16-10	QUT MULTI-CHANNEL ANALYZER (LECROY 3001)	0001
N-16-20	TIME TO PULSE HEIGHT CONVERTER (ORTEC 467)	0010
N-16-31	6-CH VOLTAGE INTEGRATOR KEK TYPE-1	0002
N-17-11	PDP-11 INTERRUPT CONTROLLER (FOR DR11-C) KEK TYPE-1	0010
N-18-11	PRINTER CONTROLLER KEK TYPE-1	0005

(2) CAMAC MODULE

	NUMBERS
C-00-11 CAMAC BLANK MODULE CASE KEK TYPE-1	
C-01-10 POWERED CRATE (SCHLUMBERGE CJAL-41)	0004
C-01-10 POWERED CRATE (SEN 2057)	0010
C-01-10 POWERED CRATE (SEN 2057-S)	0006
C-01-10 POWERED CRATE (ITC 5000)	0023
C-01-10 POWERED CRATE (ITC 5001)	0002
C-01-10 POWERED CRATE (SEC ULTIMA 3000)	0009
C-01-20 UNPOWERED CRATE (JAC JC-661)	0006
C-01-20 UNPOWERED CRATE (NE 7005)	0001
C-01-20 UNPOWERED CRATE (SCHLUMBERGE CJAL-41)	0002
C-02-10 CAMAC POWER SUPPLY (NE 9001)	0001
C-02-10 CAMAC POWER SUPPLY (JAC JC-662)	0002
C-03-10 CAMAC MODULE EXTENDER (NE 7007)	0001
C-03-10 CAMAC MODULE EXTENDER (SEC EB-01)	0004
C-03-11 CAMAC MODULE EXTENDER KEK TYPE-1	0010
C-03-11 CAMAC MODULE EXTENDER KEK TYPE-2	0004
C-04-10 CRATE CONTROLLER TYPE-A1 (EGG CC-101)	0001
C-04-10 CRATE CONTROLLER TYPE-A1 (SEN ACC2034)	0027
C-04-10 CRATE CONTROLLER TYPE-A1 (BORER 1502)	0003
C-04-10 CRATE CONTROLLER TYPE-A2 (SEC CCA2)	0002
C-04-10 CRATE CONTROLLER TYPE-A2 (SEN ACC2089)	0007
C-04-20 PDP-11 DEDICATED CRATE CONTROLLER (EGG DC011)	0002
C-04-20 PDP-8 DEDICATED CRATE CONTROLLER (NE 7048-2)	0001
C-04-20 NOVA-01 CRATE CONTROLLER (SEN CC2023)	0006
C-04-30 MANUAL CRATE CONTROLLER (SCHLUMBERGE JCMC10)	0002
C-04-30 MANUAL CRATE CONTROLLER (NE 7024-1)	0001
C-04-30 MANUAL CRATE CONTROLLER (SEC MCC-240)	0002
C-04-31 MANUAL CRATE CONTROLLER KEK TYPE-1	0005
C-04-40 PROGRAMMED PLUGBOAD TEST CONTROLLER (NE SPS2040)	0001
C-05-10 BRANCH DRIVER (FOR PDP-11) (EGG BD011)	0005
C-05-20 MANUAL BRANCH DRIVER (SCHLUMBERGE CCMB10)	0001

		NUMBERS
C-06-10	BRANCH TERMINATOR (EGG TC024)	0001
C-06-10	BUS TERMINATOR (FOR NOVA-01) (SEN BT2022)	0004
C-06-21	BRANCH TERMINATOR (WITH DISPLAY) KEK TYPE-1	0011
C-06-31	BRANCH TERMINATOR AND BRANCH HIGHWAY CABLE TESTER KEK TYPE-1	0002
C-06-40	BRANCH HIGHWAY TRANSCEIVER (SCHLUMBERGE JBHT10)	0002
C-06-40	BRANCH HIGHWAY TRANSCEIVER (GEC DBE6501)	0002
C-06-41	BRANCH HIGHWAY RECEIVER/TRANSMITTER KEK TYPE-1	0010
C-06-42	BRANCH HIGHWAY MULTIPLEX RECEIVER/TRANSMITTER KEK TYPE-2	0003
C-07-10	POWER INDICATOR (NE 704-1)	0001
C-07-11	POWER INDICATOR KEK TYPE-1	0028
C-08-10	DUAL INPUT REGISTER (NE 9041)	0001
C-08-10	DUAL INPUT REGISTER (EGG RI224)	0002
C-08-11	DUAL 24-BIT INPUT REGISTER KEK TYPE-1	0005
C-08-20	DUAL OUTPUT REGISTER (EGG RO224)	0002
C-08-21	16-BIT OUTPUT REGISTER KEK TYPE-1	0010
C-08-22	DUAL 24-BIT OUTPUT REGISTER KEK TYPE-1	0005
C-08-30	16-CHANNEL COINCIDENCE REGISTER (LECROY 2341S)	0009
C-08-31	16-CHANNEL COINCIDENCE REGISTER KEK TYPE-1	0041
C-08-32	16-CHANNEL COINCIDENCE REGISTER KEK TYPE-2	0001
C-08-33	12-CH OVERLAPPED COINCIDENCE REGISTER KEK TYPE-1	0010
C-08-41	16-BIT SWITCH REGISTER KEK TYPE-1	0025
C-08-42	24-BIT SWITCH REGISTER KEK TYPE-1	0010
C-08-50	8-BIT INTERRUPT REGISTER (NE 7013)	0001
C-08-50	8-BIT INTERRUPT REGISTER (NE EC218)	0001
C-08-50	12-BIT INTERRUPT REGISTER (EGG IR026)	0001
C-08-51	8-BIT INTERRUPT REGISTER KEK TYPE-1	0002
C-08-60	TEST MODULE (EGG TM024)	0001
C-08-60	TEST MODULE (SEN TD2040)	0002
C-08-60	TEST MODULE (SEN TM2040)	0001
C-09-10	LAM GRADER (NE 064)	0002
C-09-11	LAM GRADER KEK TYPE-1	0030
C-10-10	QUAD BCD 20MHZ SCALER (NE 9021)	0001
C-10-11	QUAD BINARY 60MHZ SCALER KEK TYPE-1	0015
C-10-12	QUAD BINARY 80MHZ SCALER KEK TYPE-2	0080
C-10-20	PRESET COUNTING REGISTER (NE 7039)	0001
C-11-10	OCTAL ANALOG TO DIGITAL CONVERTER (LECROY 2248)	0002
C-11-10	12-CH ANALOG TO DIGITAL CONVERTER (LECROY 2249A)	0026
C-11-10	12-CH ANALOG TO DIGITAL CONVERTER (LECROY 2249W)	0002
C-11-10	32-INPUT DIFFERENTIAL A-D CONVERTER (LECROY 2232)	0005
C-11-10	1024-CH ANALOG TO DIGITAL CONVERTER (SCHLUMBERGE JCAN40)	0001
C-11-20	OCTAL TIME TO DIGITAL CONVERTER (LECROY 2228A)	0043
C-11-21	OCTAL TIME TO DIGITAL CONVERTER KEK TYPE-1	0010

	NUMBERS
C-12-11 10MHZ CLOCK PULSE GENERATOR KEK TYPE-1	0010
C-12-20 DELAYED PULSE GENERATOR (NE 7045)	0001
C-13-10 TTY/CRT INTERFACE (SEC TCO-100)	0002
C-13-11 NIM-CAMAC SCALER INTERFACE KEK TYPE-1	0017
C-13-20 QVT-CAMAC INTERFACE (LECROY 2301)	0001
C-14-11 DUAL FANOUT KEK TYPE-1	0030
C-15-10 MEMORY BUFFER (256 X16 B/W) (SCHLUMBERGE JMT 20)	0001
C-16-10 PROGRAMMABLE DELAY UNIT (SEN 2PD-2048)	0003
C-16-20 PROGRAMMABLE ATTENUATOR (SEN 2PD-2049)	0002

(3) ACCESSORY EQUIPMENT FOR NIM AND CAMAC MODULE

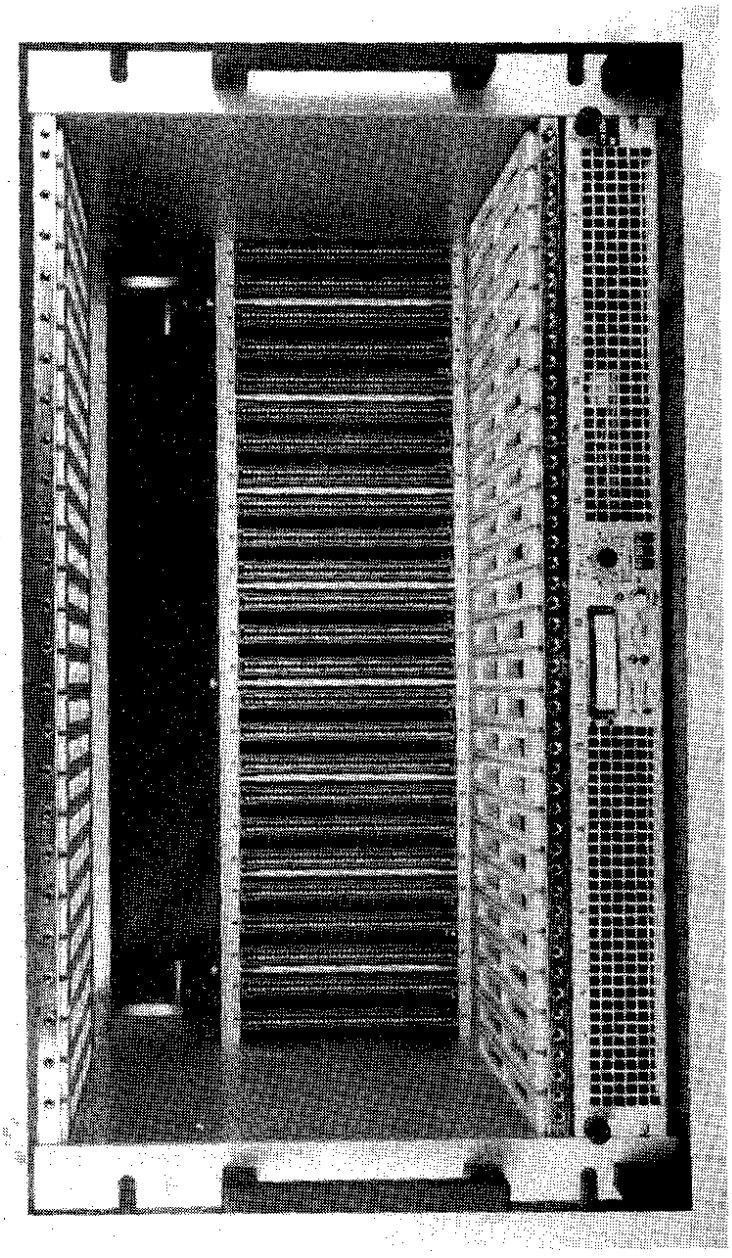
A-01-11 BNC CONNECTOR SIGNAL CABLE (RG-58C/U)
A-01-21 LEMO CONNECTOR SIGNAL CABLE (RG-174/U)

A-02-11 BNC 50-OHM TERMINATOR
A-02-21 LEMO 50-OHM TERMINATOR

A-03-11 POWER SUPPLY CABLE FOR NIM BIN (9P)
A-03-21 DATAWAY CABLE FOR NIM-CAMAC INTERFACE (50P)
A-03-31 CAMAC BRANCH HIGHWAY CABLE (132P)
A-03-41 CAMAC LAM GRADER CABLE (52P)

R

C01-10 POWERED CRATE (SEN 2057S)



KEK CAMAC STANDARD (C01-10)
CAMAC POWERED CRATE (SEN-PC2057)

KEK CAMAC STANDARD MODULE (C01-10)
POWERED CRATE (SEN 2057-S)

This crate conforms to all EUR CAMAC specifications, but incorporates several new features (required by CERN Document 46-02). Principally, the ventilator chassis and power supply can now be withdrawn easily without having to remove the crate from the rack.

SPECIFICATIONS

Input Voltage

220 V + 10 %, - 12 % at 50 Hz, ± 3 Hz.

DC Outputs (max combined power - 300 W)

+ 6.0 V	-	32 Amps	Stabilized and meter monitored.
- 6.0 V	-	32 Amps	Impedance less than 0.3 Ohms.
+ 24.0 V	-	6 Amps	Ripple less than 2 mV rms.
- 24.0 V	-	6 Amps	

The total combined current of the 6.0 V outputs is limited to 35 Amps.

Protection

Inputs fused, and all outputs protected against short-circuit.
Overheating prevented by thermal switch.

The ± 6 V and ± 24 V outputs are adjustable.

Indicator Lamps

Green LED	-	Status; is on when supply functions correctly.
Yellow LED	-	Fan failure.
Orange Neon	-	AC power on.
Red LED	-	Short Circuit or Overload.
Yellow LED	-	Activated by the thermal switch at 55° C.

Audio alarm fitted.

Power Supply

The unit is totally enclosed by an integrated metal electrostatic shield which incorporates a heat sink and single fan ventilator. The unit slides in and out on bearing strips fitted with an automatic lock. All circuits are on plug-in printed cards, and there is no conventional wiring except to the 75 pin AMP connector and the monitor socket.

INSTALLATION

The PC 2057 S is designed for mounting in a standard 19" rack, and all mechanical specifications conform to CERN report CIM N° 25543, as well as EUR 4100.

Before connecting to the mains supply, please double check that this corresponds to the input specifications of the crate. Full specifications are given on the back of the power supply unit.

The ON/OFF switch is self-locking. The lever has to be pulled outwards to disengage the lock before being moved to either position.

The Indicator Lamps on the front panel should be checked after the first, and any subsequent, installation.

The CLEAN EARTH connection to the dataway is made by bridging the two 4 mm. banana sockets at the rear of the power supply unit (see component location diag.).

The 'OVERLOAD' and 'OVERHEAT' LEDs will light up momentarily when the crate is switched on or off. During normal operation they will remain unlit.

The Alarm Buzzer can be disabled, if required, by activating a switch which is accessible once the ventilator sub-chassis has been removed.

The Main Input is cut off automatically by Rel. 1 when the output dissipation exceeds 300 W.

FITTING CAMAC MODULES

It is most important that modules are always correctly installed in order to avoid damaging the dataway connectors.

a) Holding the module by the front panel, with one hand at the top and one at the bottom, align it with the required station(s).

b) Keeping the module vertical, push it into the crate slowly and firmly until the connector is fully engaged.

c) Tighten the retaining screw at the bottom with one hand, while maintaining a continuous pressure at the top with the other.

CURRENT AND VOLTAGE ADJUSTMENTS

The colour-coded meter and 12 position switch on the front panel provide a continuous check on both current and voltage while the crate is in operation. The accuracy of the meter should be checked after installation, and after any subsequent component changes.

The four regulated voltages ($\pm$ 6 V and $\pm$ 24 V) can be adjusted by the potentiometers marked 'U' on the regulating circuits (see component location diag.).

The current readings of the front panel meter can be checked and adjusted in the following manner :

a) Connect a known resistance accross each voltage supply

b) Check the meter readings

c) To remove any discrepancies, adjust the potentiometers marked 'Meter 1' on each regulating circuit (see component location diag.).

REMOTE MONITORING

The 'MONITOR' socket at the rear of the power supply unit provides for remote monitoring of the crate by a computer or other device, and covers the following functions :

- The four regulated voltages are monitored at their nominal value
- A power failure output. Signal output levels conform to the CAMAC specifications (i.e. 15 mA '1', indicating a warning ON condition)
- A status monitor. (When the power supply works properly : relay contacts closed). The status bit is reset by a rearment input signal
- One rearment input signal (24 V).

MALFUNCTIONS

'OVERLOAD' - Front Panel LED
'STATUS' - Front Panel LED

A variety of malfunctions will activate the overload LED, and switch off the 'STATUS' LED, but by using the meter to check out voltage and current levels, the operator will be able to identify the cause of the trouble from the table below. Unless previously disabled, the alarm buzzer will also function while the LED 'status' is off.

'STATUS' LED off - 'OVERLOAD' LED on

Volts	Amps	Cause	Remedy
nominal	exceeds nominal	overload	reduce the current drain by removing defective or excess modules.
zero	approx. 3A for ± 6V 1.5A for ± 24V	overvoltage short-circuit	1. Can be caused by momentary internal or external parasites. Switch off the crate, then switch on again after a few seconds. 2. If malfunction persists, there is a short-circuit. Switch off the crate - check dataway connectors first.
zero power supply cut	zero	excess power used	reduce the power consumption by removing any defective or excess modules.
intermittent power ± 6V and ± 24V		circuit over-heating	1. Check that power supply grill is not obstructed. 2. Check power supply fan is operating. 3. Check that mains supply does not exceed specified voltage by more than 10%. 4. Check that the regulating circuit concerned is not producing more than the nominal current and overheating the ballast transistor.

'OVERHEAT' - Front Panel LED

This indicates that the ambient temperature is too high.

At 55° C and over	LED and buzzer on continuously. A thermal switch cuts off the primary supply to the transformer.

The only remedy is to improve the ventilation of the rack in particular, and/or the laboraroy as a whole.

CONTROL CIRCUIT

The Control Circuit contains two power supplies, the + 12 V and - 6 V, which are completely independent of all other power sources. They can be adjusted by the potentiometers P1 and P2, marked '+ 12 V aux' and '- 6 V aux'.

The potentiometer P6 * can be adjusted in order to change the sensitivity of the 'Power Fail' circuit : this is correctly set when the voltage drops to zero on pin N° 12 of the 'MONITORING' connector, with a mains voltage of 180 to 185 V. Turning anti-clockwise reduces the sensitivity of the circuit.

The comparator 5 detects any anomalies occuring on the four regulated CAMAC voltages (6 for 450 NIM) : in order to regulate the comparator, all voltages must be correctly adjusted and available on the dataway. Adjust P5 so as to have - 30 mV at the second test point, and P7 to have + 30 mV at the first test point - the status LED should be 'on'.

Reset the bistable 6 to zero using a 24 V x 20 mA rearment signal on pins 34 and 35 of the monitor connector. The status relay contacts (pins 11 and 23 of the monitor connector) should be closed.

Although the STATUS and OVERLOAD LEDs will be alternatively activated by an intermittent fault, the STATUS data available on pins 11 and 23 of the monitor connector will remain in the 'bad' state after the first occurence of the fault since the bistable 6 memorises this condition. In order to reset this bistable, a rearment signal has to be sent on pins 34 and 35 of the monitor connector.

If the fault was the result of a temporary overvoltage, the power supply can be restarted by sending two successive rearment signals without touching the main ON-OFF switch : this provides for remote operation of the crate during difficult working conditions. The first signal re-starts the crate and the second sets the STATUS relay in the 'good' state.

When the crate is switched on, it may be necessary to reset the bistable to zero in order to set the STATUS relay correctly.

FAN FAILURE CIRCUIT VM 2057 S and 2085

The ventilation sub-chassis has an independent electronic circuit which detects a failure of any of the three fans, or an unusual rise in temperature due to blocked air intakes. When the 'FAN FAILURE' LED comes on, the main transformer is disconnected from the mains supply. If the circuit is found to be over-sensitive, the potentiometer should be turned in a clock-wise direction.

If, for any reason, the user wishes to suppress the safety circuit which cuts off the main transformer, but retain the visual facility of the 'FAN FAILURE' LED, it is simply a matter of repositioning the AMP fast-on connector on the printed circuit 1480 S.

P MAX CIRCUIT

The potentiometer provides adjustment of the maximum power output level : turning anti-clockwise raises the level. If this level is exceeded, Relay 1 cuts off power to the main transformer T1 and only the two auxiliary supplies remain operational.

Adjustment procedure ± 24 V, + 6 V, - 6 V (± 12 V NIM)

Each regulator circuit has :

P1 - Current limiter adjustment.
This potentiometer should be adjusted so that the current limiter trips ('Overload' LED comes on) at 110 % of the maximum specified load.

P2 - Short-circuit current adjustment.
The potentiometer is adjusted so that, when a short-circuit exists at the output of the regulating circuit, the current passing through the circuit does not exceed 1.5 A for the ± 24 V (and ± 12 V), and 4 A for the ± 6 V. When one of the regulators discharges into a short-circuit, the 'Overload' LED comes on.

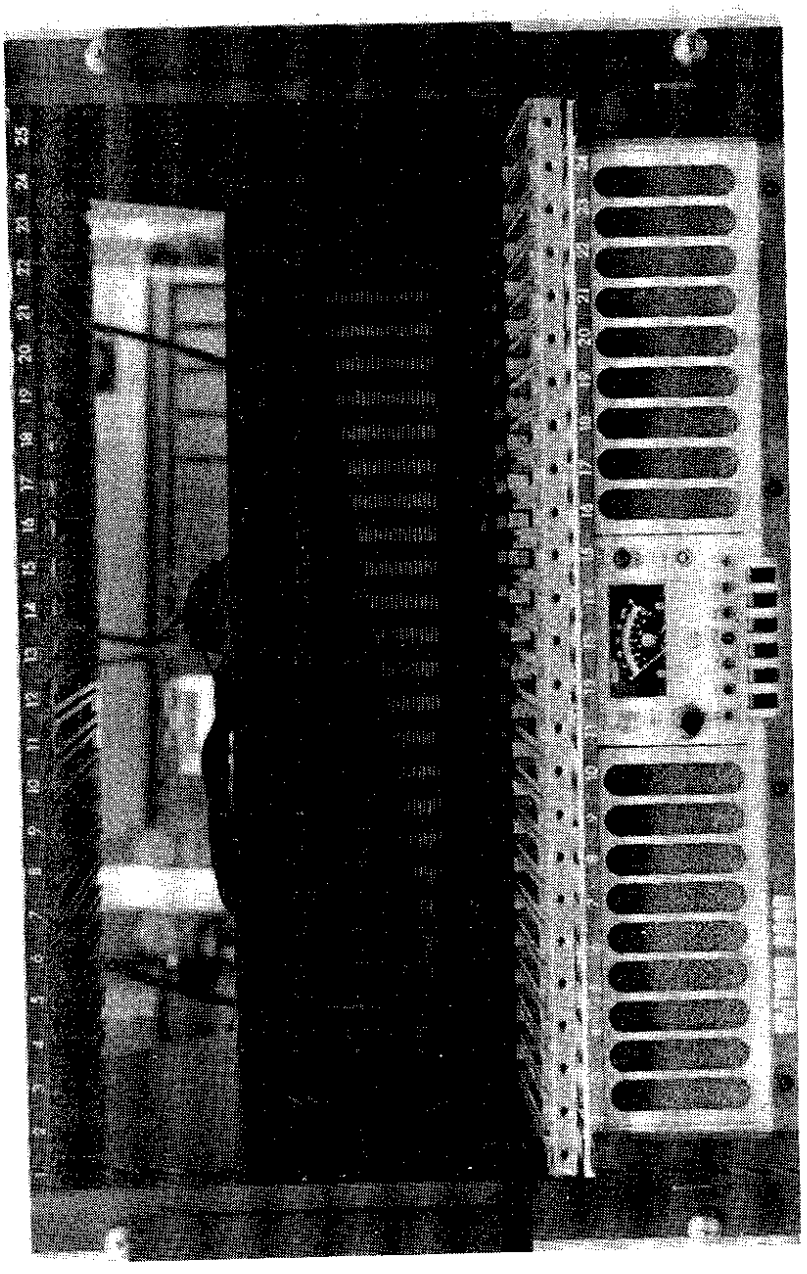
P3 - Overvoltage cut-out adjustment. (2085 on the motherboard)
The potentiometer is set so that the maximum voltages on the dataway do not exceed 20 % of the nominal values. (see specifications).
An overvoltage produces a short-circuit at the regulator output through a thyristor, and consequently activates the current limiter.
In order to return to normal operation it is necessary to :

i) switch off the crate.
ii) identify and remove the cause of the overvoltage.
iii) switch on the crate again.

P5 - Meter current adjustment.

P6 - Output voltage adjustment.

C01-10 POWERED CRATE (SEC ULTIMA 3000)



KEK CAMAC STANDARD MODULE (C01-10)
POWERED CRATE (SEC ULTIMA3000)

KEK CAMAC STANDARD MODULE (C01-10) C01-10-01
POWERED CRATE (SEC ULTIMA 3000)

GENERAL

The Ultima 3000 has been designed for long reliable operation under adverse conditions. The unit is comprised of an easily removable power supply and the CAMAC crate with its slide in blower drawer. The Crate and Power Supply meet or exceed the applicable parts of CAMAC specification EUR4100e and AEC TID-25875.

(1) The CAMAC Crate and Blower

The CAMAC crate is of rugged construction utilizing 3/16 inch thick aluminum side panels to maintain proper crate alignment. The Dataway is of the proven "Berkeley" type multilayer motherboard utilizing low insertion pressure edge connectors and heavy duty copper bus bars for all power distribution. The grills are made from NC machined, nickle plated cast aluminum in order to provide the degree of precision alignment required for CAMAC.

The easily removable blower drawer (finger latch release) has been designed with air baffles and anti-vibration and acoustic noise dampeners to provide adequate air flow even if a crate is only 1/3 loaded with modules. Air filters are provided and are easily removable for cleaning.

The blower also contains all metering elements, power switch and associated contactor, and voltage monitor option.

(2) The Power Supply

The performance of the power supply meets or exceeds the requirements of CP-1 Power Supply and ESONE report EUR-4100e. It is contained in an easily removable, ruggedly constructed aluminum housing and is capable of providing 375 watts from any combination of the ±6 V, ±12 V (optional) and ±24 V outputs consistent with their current limitations.

The power supply is of modular construction to maximize ease of maintenance. The electronic circuit regulators are contained on a single printed curcuit board and all the series pass transistors and associated components are contained on an easily removable heat sink. Internal fuses can be seen from the outside through a window.

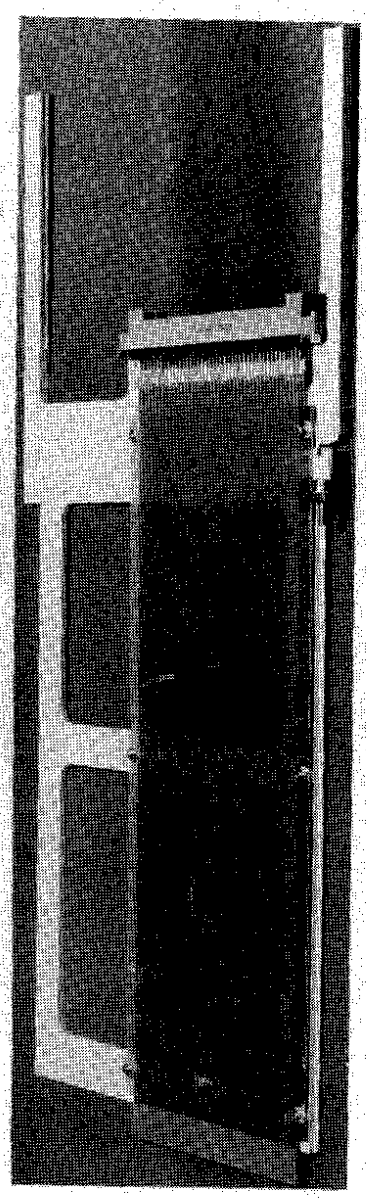
Overvoltage and overcurrent protection are provided on both the ±6 V and ±24 V outputs. The overcurrent settings and output voltage settings are easily achieved through access holes in the rear cover.

Over temperature sensing is provided to protect the power supply should the internal temperature exceed safe limits.

SPECIFICATIONS

Crate name : ULTIMA 3000.
Input : 100 V. 57 to 63 Hz.
Output : Max. Output 375 Watts @ 25°C.
42A@+6V, 25A@-6V > Current Shared.
6A@+24V, 6A@-24V > Current Shared but limited to total 9A.
Regulation : Better than ±0.5% for 42 Amp @+6V and ±0.2% for 24 V over 24 hour period.
Stability : ±0.5% for ±6 V.
±0.3% for 24 V over 6 month period.
Noise & Ripple : Less than 12 mv. peak to peak over 50 MHz bandwidth.
Temperature Range : 0 to 50°C Input Air.
Temperature Coefficient : .02%/°C.
Voltage Adjustment Resolution : Better than ±0.2%.
Transient Recover Time : Less than 0.5 ms. to 0.2%.
Overload Protection : Fold back current limiting, all outputs.
Crowbar : ±6V, 7.5V Max..
±24V, 34V Max..
Status Monitoring : Monitors thermal overload and all four voltages.
External Voltage Measurement : Tip jacks on front panel.

C03-11 CAMAC MODULE EXTENDER (KEK TYPE-1)



KEK CAMAC STANDARD (C03-11)
CAMAC EXTENDER KEK TYPE-1

KEK CAMAC STANDARD MODULE (C03-11)
CAMAC MODULE EXTENDER KEK TYPE-1

GENERAL

This CAMAC module extender is a single width extension unit that plugs into a CAMAC crate and is fitted with extension guides in front of the CAMAC crate.

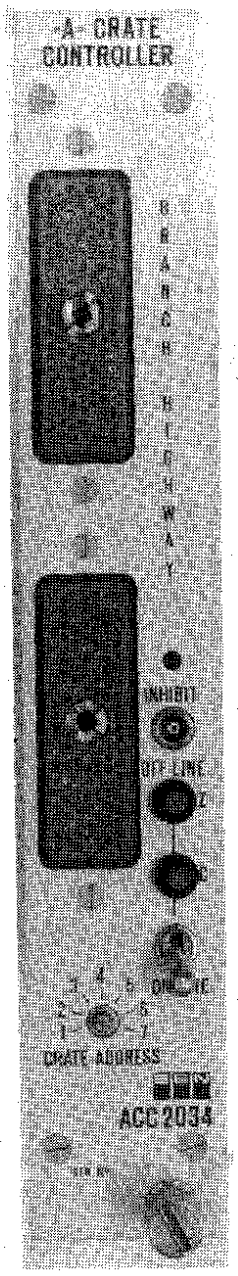
A standard dataway edge connector (86-pin) is mounted at the rear of the extension guides thus enabling CAMAC modules to be connected to the dataway, while in front of the CAMAC crate for maintenance and testing purposes.

It can be plug a module of multiple print boards by using plural units.

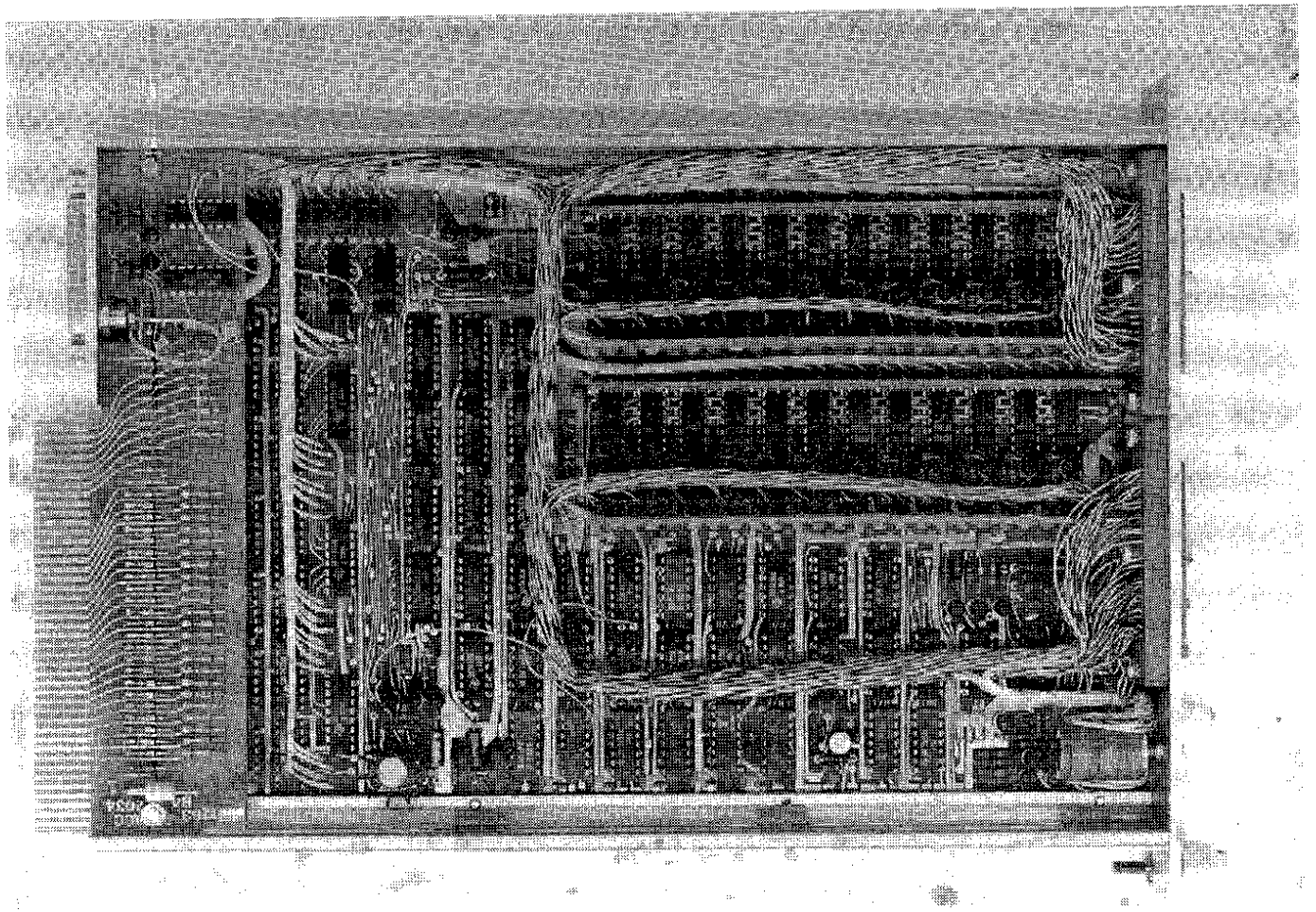
SPECIFICATIONS

Connector : PCBD43N771E00 (86-pin).

C04-10 CRATE CONTROLLER TYPE-A1 (SEN ACC 2034)



KEK CAMAC STANDARD MODULE (C04-10)
CRATE CONTROLLER TYPE-A1 (SEN ACC2034)



(INSIDE VIEW)
CRATE CONTROLLER TYPE-A1 (SEN ACC2034) (C04-10)

KEK CAMAC STANDARD MODULE (C04-10)
CRATE CONTROLLER TYPE-A1 (SEN ACC 2034)

SPECIFICATIONS

(1) OUTSTANDING FEATURES

- Only one printed circuit board (increases fiability, and keeps down price) facilitates test and maintenance.
- The second dataway connector is independent of the first, allowing easy plugging into the crate.
- Synchronous logic (timing accuracy).
- CAMAC cycle is not disturbed by parasite pulses.
- Master clock started by the branch driver and controlled by the Hold Line (CERN option).
- Variable frequency clock with only one adjustment.
- CAMAC cycle typical 1 μs.
- Complete decoding of functions and sub-addresses.
- X-response for each function decoded in the Crate Controller.
- The branch highway is not disturbed by a connected but unpowered ACC 2034.

(2) CAMAC FUNCTIONS

ADDRESS N28 (with S1; S2; B).

F(26) A(8) : Generate Dataway Z →BQ=0.
F(26) A(9) : Generate Dataway C →BQ=0.

ADDRESS N30 (with S1; S2; B).

F(0) A(0-7): Read GL →BQ=1.
F(16) A(8) : Load SNR →BQ=1.

F(24) A(9) : Remove Dataway I →BQ=0.
F(26) A(9) : Set Dataway I →BQ=0.
F(27) A(9) : Test Dataway I →BQ=1 if I=1.

F(24) A(10): Disable BD Output →BQ=0.
F(26) A(10): Enable BD Output →BQ=0.
F(27) A(10): Test BD Output →BQ=1 if BD enabled.

F(27) A(11): Test Demand Present →BQ=1 if demands present.

STATION NUMBER CODES

N1 to N23:	Address one normal Station.
N24:	Address preselected normal Stations.
N26:	Address all normal Stations.
N28:	Address crate controller only.
N30:	Address crate controller without S1; S2; B.
N0; 25; 27; 29; 31:	Are reserved.

All CAMAC functions used here give BX=1.

(3) GENERAL

Front Panel Commands

Crate Address: 7 position switch allows selection of the addresses BCR 1 to 7 of the "A" Crate Controller.

ON LINE/OFF LINE, Links the Crate Controller to the Branch Driver.

Initialize (Z): This push button sends Z signal in position OFF LINE.

Clear (C): This push button sends C signal in position OFF LINE.

INHIBIT (I): LEMO RA-00-C50 Connector. Accepts I signal with TTL level.

PHYSICAL

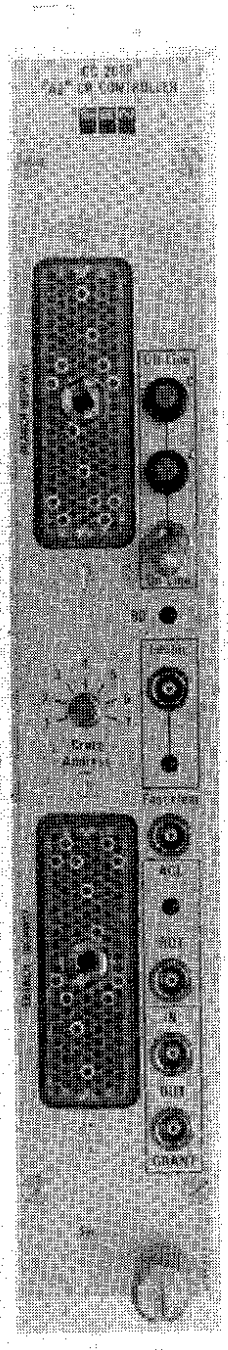
Double width CAMAC module with shield covers on both sides. Fiber-glass printed circuit board with plate-through holes.

Meets elecrical and mechanical requirements of EUR 4100e and 4600e.

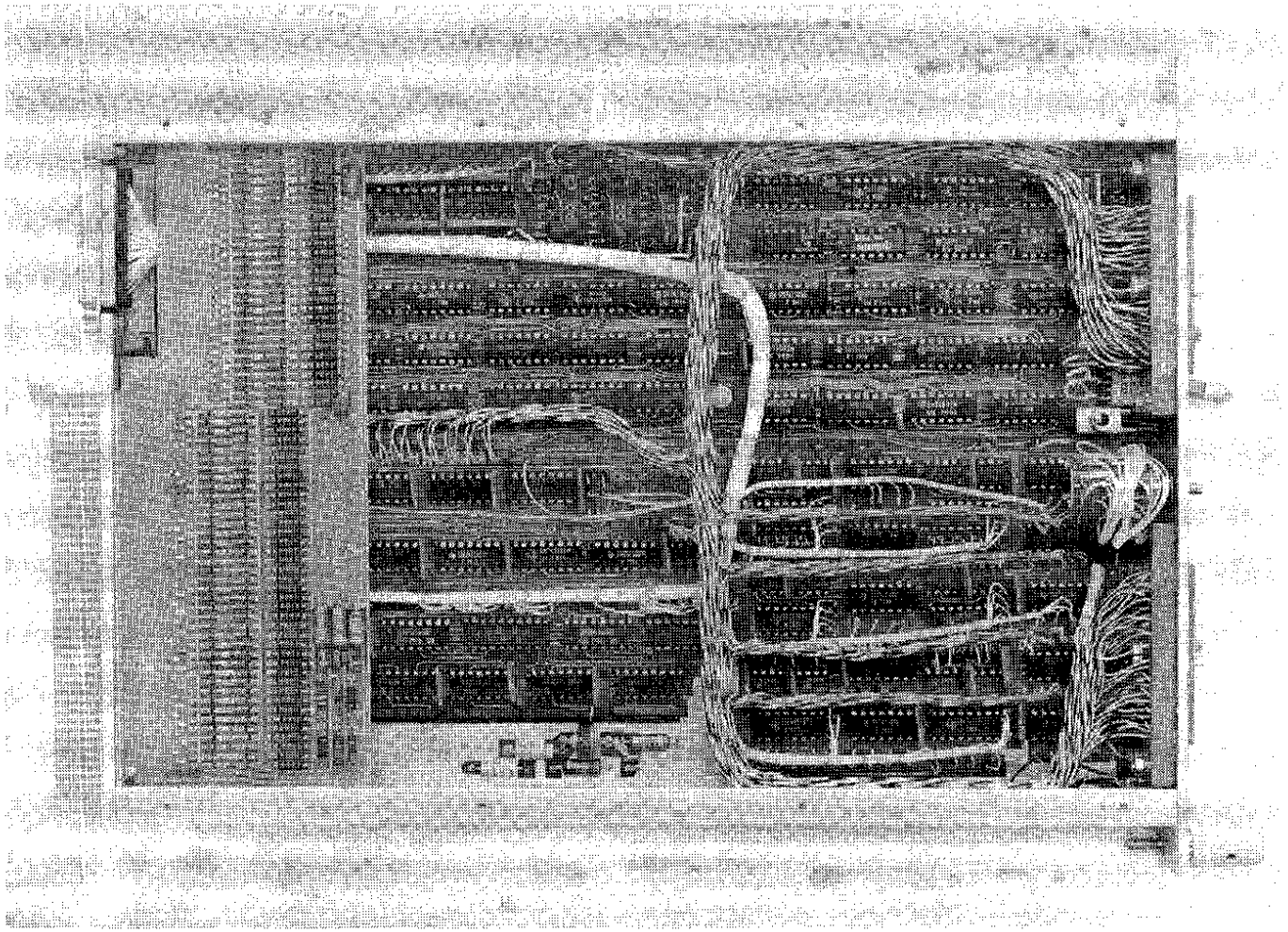
POWER REQUIREMENTS

+6V at 2.4A.
-6V at 100mA.

C04-10 CRATE CONTROLLER TYPE-A2 (SEN ACC 2089)



KEK CAMAC STANDARD MODULE (C04-10)
CRATE CONTROLLER TYPE-A2 (SEN ACC2089)



(INSIDE VIEW)
CRATE CONTROLLER TYPE-A2 (SEN ACC2089) (C04-10)

GENERAL

The A2 Crate Controller has been developed from the earlier A1 unit and has all the same functions plus new control logic for local data handling using a microprocessor. The A2 provides access to the N and L lines, via a rear panel connector, for an intelligent module placed in any normal station. It also handles the remote/local access request conflicts.

Front-end data processing is governed by this module just as long as the main computer does not require access to this particular crate: however, when this occures, the local processor is released and its status saved. Subsequently the Branch demand is processed. Once the Branch demand has been filled, control returns to local processing. This mode is the normal working mode and is called the request/Grant mode. Another mode, called the Auxiliary lock-out mode, can be implemented: when selected all the local processing is inhibited until the Request/Grant mode is again selected.

The CC2089 features a single PC board design which increases flexibity and facilitates test and maintenance. It also includes a fast clear entry which allows distribution of a clear signal on the dataway at the crate controller (particularily convenient for pattern units, ADC, TDC etc. ...). Two led's are mounted on the front panel: one displays the ACL mode, the other indicates a branch demand.

SPECIFICATIONS

(1) Functions

ADDRESS N28 (with S1; S2; B)

F(26)A(8) : Generate Dataway Z, BQ=0
F(26)A(9) : Generate Dataway C, BQ=0

ADDRESS N30 (with S1; S2; B)

F(0)A(0-7) : Read GL, BQ=1
F(16)A(8) : Load SNR, BQ=1
F(24)A(9) : Remove Dataway I, BQ=0
F(26)A(9) : Set Dataway I, BQ=0
F(27)A(9) : Test Dataway I, BQ=1 if I=1
F(24)A(10) : Disable BD Output, BQ=0
F(26)A(10) : Enable BD Output, BQ=0
F(27)A(10) : Test BD Output, BQ=1 if BD enabled
F(27)A(11) : Test Demand Present, BQ=1 if demands present

STATION NUMBER CODES

N1 to N23 : Address one normal Station

N24 : Address preselected normal Stations C04-10-02
N26 : Address all normal Stations
N28 : Address crate controller only
N30 : Address crate controller without S1; S2; B
NO; N25; N27; N29; N31 : reserved

All CAMAC functions used here give BX=1

(2) Front panel

Crate Address : 7 position switch allows selection of the addresses BCR 1 to 7 of the "A" Crate Controller.
ON LINE/OFF LINE : Links the Crate Controller to the Branch Driver.
Initialize(Z) : This push button sends Z signal in position OFF LINE.
Clear(C) : This push button sends C signal in position OFF LINE.
INHIBIT(I) : LEMO RAOO C50 connector. Accepts I signal with TTL level.
Request(RQ) : LEMO RAOO C50 connector: Indicates RQ signal; TTL level.
Grant IN(GI) : LEMO RAOO C50 connector: Accepts RQ signal output, or other signals according to the priority order; TTL level.
Grant OUT(GO) : LEMO RAOO C50 connector: Outputs GO signal (TTL) to the next Grant IN input.
BD LED : LED indicating a branch demand.
ACL/RG LED : LED indicating Request/Grant mode or Auxiliary Controller lockout (ACL). On when in ACL mode.
Fast Clear : LEMO RAOO C50 connector; TTL level.

(3) Rear panel

LAM Grader Connector : 52 pin, double-density Cannon.
Auxiliary Controller BUS (ACB) Connector : 40 pin AMP.

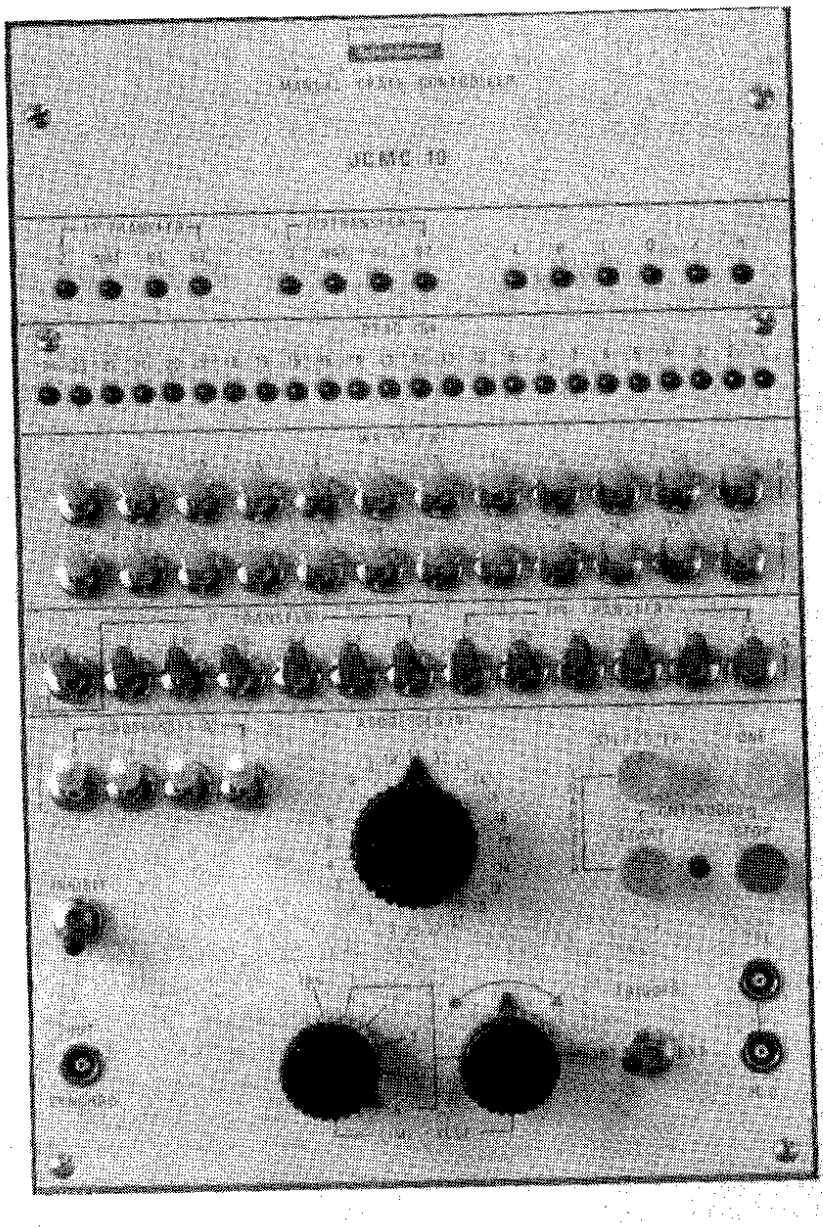
(4) Physical

Meets electrical and mechanical requirements of EUR 4100e, 4600e and 6500e.

(5) Power requirements

+6V : 3A
-6V : 150mA

C04-30 MANUAL CRATE CONTROLLER (SCHLUMBERGE JCMC 10)



KEK CAMAC MODULE (C04-30)
MANUAL CRATE CONTROLLER

KEK CAMAC STANDARD MODULE (C04-30) C04-30-01
MANUAL CRATE CONTROLLER (SCHLUMBERGE JCMC10)

GENERAL

This module has been designed to control and check CAMAC dataway signals. CAMAC (N.A.F) functions can be generated for which R (read) line status is displayed and W (write) line data set by switches on the front panel. For each trigger signal, the module executes one or two consecutive dataway transfers and generates a timing signal efficient means of cheking CAMAC modules plugged into a standard CAMAC crate.

CHARACTERISTICS

(1) Programming of CAMAC functions

The function (F) and subaddress (A) are programmed by switches as well as Z, C and I. The station address is selected by means of a rotary switch.

There is a set of switches (F) for each of the two consecutive transfers — More over the first transfer can be an initialisation (Z) and second one a clear (C) — The first transfer can be enabled or disabled with a switch.

A set of 24 switches determines the state of the W lines.

24 lamps display the state of R lines.

14 lamps display the state of following signals:

(a) Z, NAF, S1, S2 for first transfer.
(b) C, NAF, S1, S2 for second transfer.
(c) I, B, L, Q, X and H.

(2) Transfer triggering

(a) Manual triggering

* Step by step: push-button can be used to execute step by step the sequence NAF, S1, S2, reset.
* Single transfer: the command is triggered by means of push-button, the sequence NAF, S1, S2 is generated according to an internal oscillator. There are one or two transfers depending on the position of the switch associated with the first transfer.
* Continuous transfer: CAMAC cycles are triggered according to the internal oscillator frequency selected. Two push-buttons provide "start-stop" control.

(b) External signal triggering

* Two inputs:
  "50 ohms" for terminated CAMAC signals.
  "TTL" for unterminated CAMAC signals.

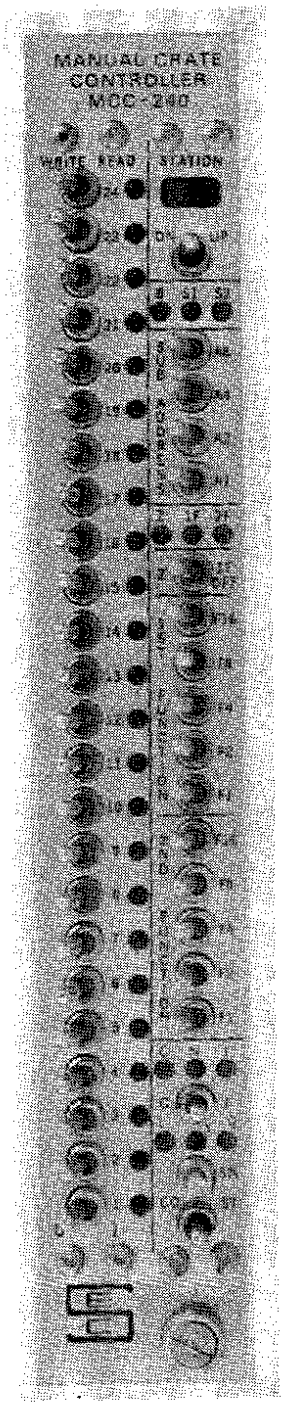
(3) Transfer duration C04-30-02

(a) The internal oscillator determines the duration and the frequency of the transfer (dataway cycle).
(b) By means of a switch and potentiometer the transfer duration can be set to 1µs (fixed by delay line) or adjusted from 0.8µs to 10ms in 5 steps with full adjustement on each range.

(4) Power requirements

+6V : 1.8A.

C04-30 MANUAL CRATE CONTROLLER (SEC MCC-240)



KEK CAMAC STANDARD MODULE (C04-30)
MANUAL CRATE CONTROLLER (SEC MCC-240)

KEK CAMAC STANDARD MODULE (C04-30)
MANUAL CRATE CONTROLLER (SEC MCC-240)

GENERAL

The SEC MCC-240 manual crate controller is a double width CAMAC module and incorporates all features necessary to control or monitor the CAMAC dataway.

CHARACTERISTICS

(1) Programming of CAMAC functions

The F(function), A(subaddress), W(write data), Z(initialize), C(clear) and I(inhibit) are selected by corresponding toggle switches on the front panel. The station number is selected electronically by a "UP-DN" slew switch and is displayed with numeric LED. The read(R) data and other CAMAC status (Q, X, L, ...) are displayed by LED's. Two CAMAC functions are generated when "1F OFF" switch is not selected. When "1F OFF" switch is selected, the first function is inhibited and the blank cycle is substituted.

(2) Operating mode

There are three types of operating mode single, step and continuous modes. The lowermost toggle switch on the front panel selects among the three modes.

"CO" : The controller will alternately generate 1 st/blank and 2 nd function continuously.
"ST" : Moving the momentary right (spring return) to the "ST" position cause the controller to step forward the sequence of CAMAC cycle, S1, S2 and blank. Each step is indicated by the appropriate LED's.
"SN" : By pushing "SN" switch when the mode-select switch is in the center position, the controller generates a single CAMAC cycle.

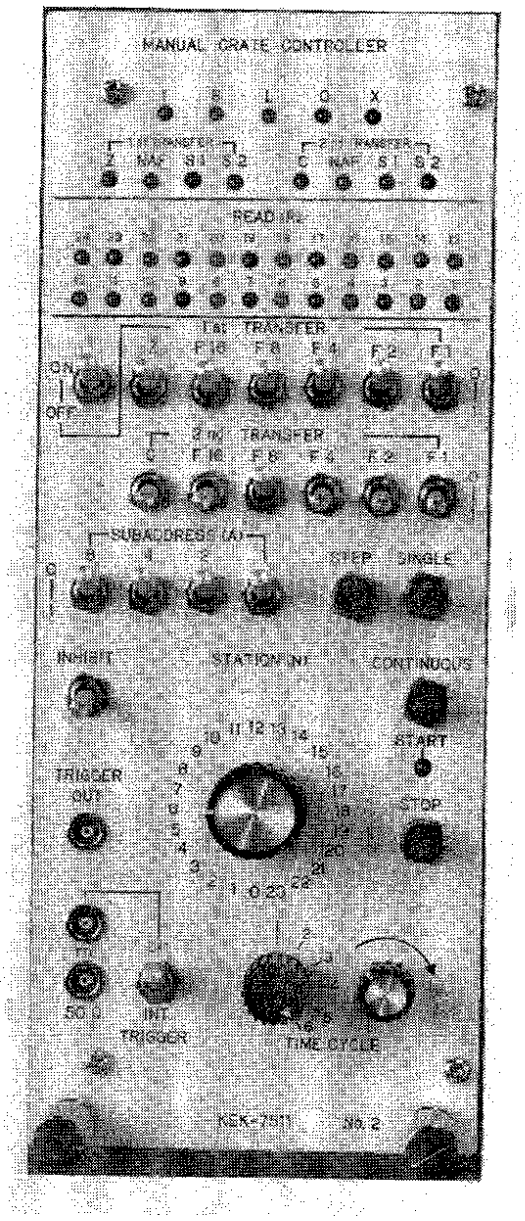
(3) Power requirement

+6 Volts : 1.6 A.

(4) Mechanical

Double width CAMAC standard module.

C04-31 MANUAL CRATE CONTROLLER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C04-31)
MANUAL CRATE CONTROLLER KEK TYPE-1

KEK CAMAC STANDARD MODULE (C04-31) C04-31-01
MANUAL CRATE CONTROLLER KEK TYPE-1

GENERAL

This module has been designed to read and check CAMAC modules plugged into a standard CAMAC crate. For each trigger signal (push button or external trigger signal), the module executes one or two consecutive dataway transfers. General specifications are almost the same as "MANUAL CRATE CONTROLLER C04-30" except that this module does not have "WRITE" function.

CHARACTERISTICS

(1) Programming

F(function), A(subaddress), Z(initialize), C(clear) and I(inhibit) are selected by corresponding toggle switches and N(station number), by a rotary switch on the front panel. LED's on the upper part of the front panel display 24 R-lines and other CAMAC status (I, B, L, Q, X, Z, C, NAF, S1, S2). Two CAMAC functions are generated when the toggle switch associated with "1 st TRANSFER" is "on". When it is "off", the 1 st function is inhibited and the blank cycle is substituted.

(2) Operating modes

(a) Manual Operation
Step : Each sequence of the CAMAC function — NAF, S1, S2, reset — is generated step by step.
Single : One or two CAMAC function is generated.
Continuous : CAMAC function is generated continuously in the selected frequency (stated in (3)).

(b) External Operation
The "TRIGGER" switch on the lower part of the front panel enables external trigger mode. Following two types of external inputs exist.
TTL : Unterminated CAMAC signal (TTL).
50 ohms : NIM logic signal.

(3) Transfer duration

The internal oscillator determines the duration and the frequency of the transfer (dataway cycle). A rotary switch and potentiometer at the bottom of the front panel changes the duration from 0.8 μsec to 10 msec.

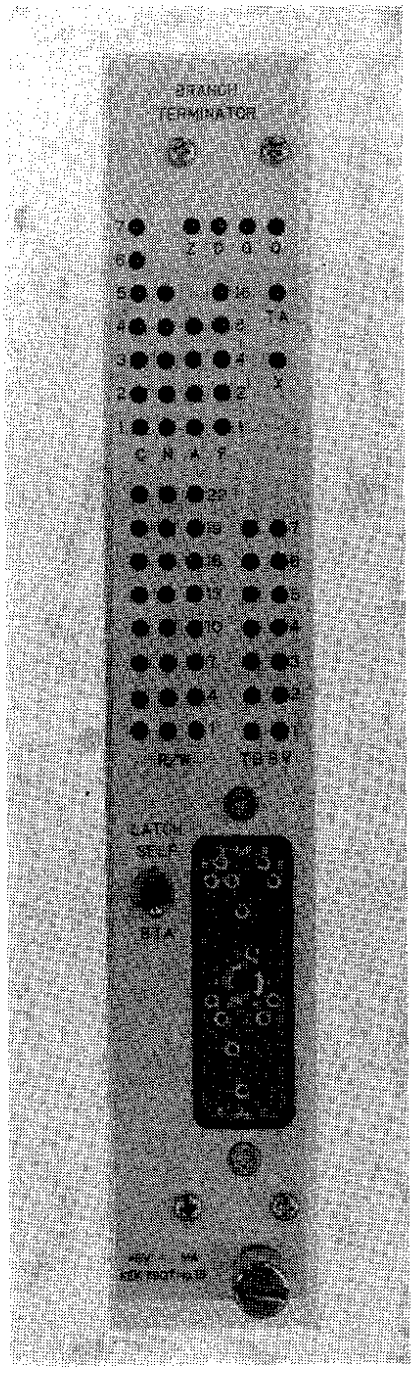
(4) Power requirement

+6 Volts : 450 mA.
-6 Volts : 34 mA.

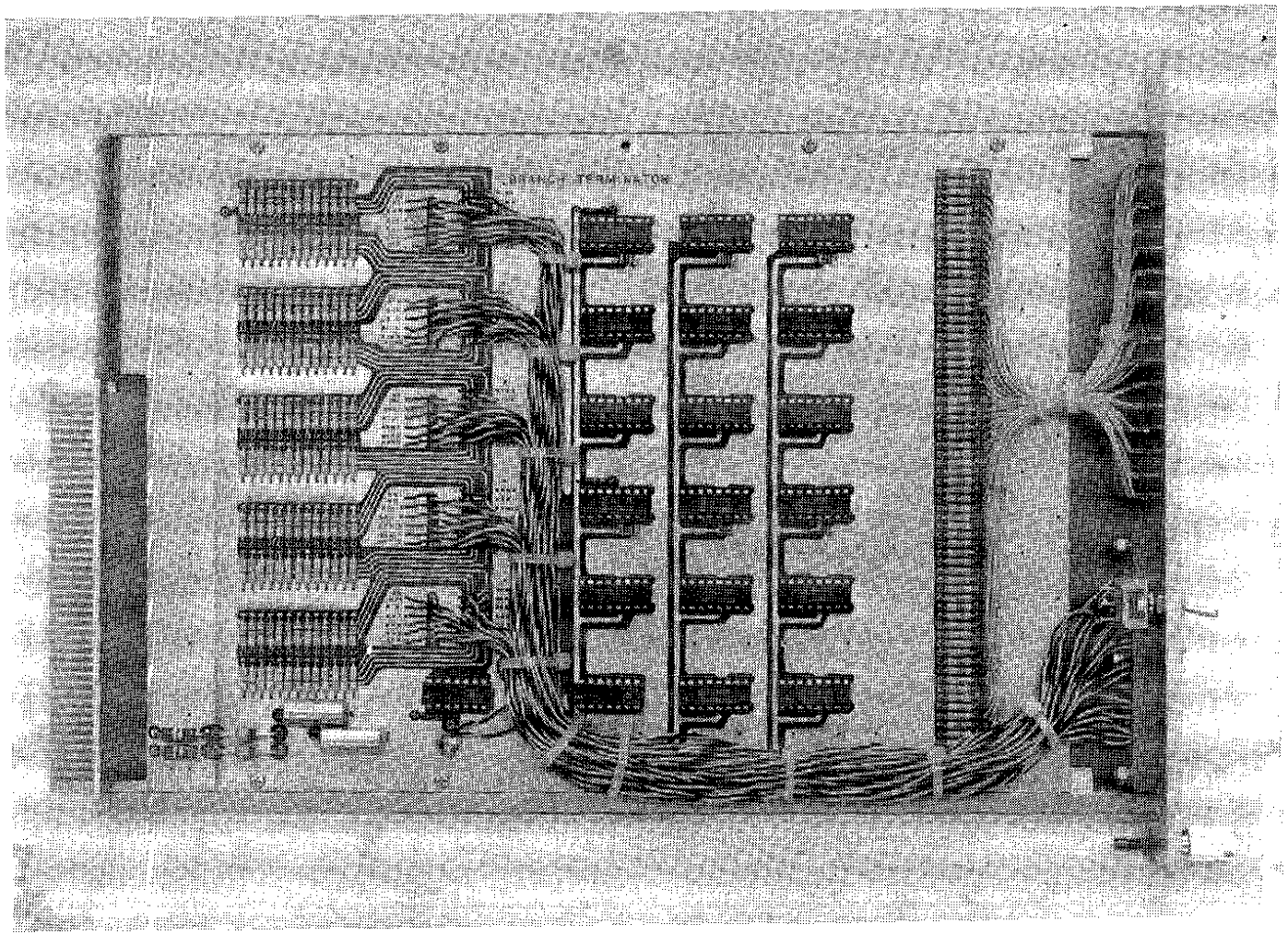
(5) Mechanical

Quintuple width CAMAC standard module.

C06-21 BRANCH TERMINATOR (WITH DISPLAY)(KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C06-21)
BRANCH TERMINATOR (WITH DISPLAY) KEK TYPE-1



(INSIDE VIEW)
BRANCH TERMINATOR (WITH DISPLAY) KEK TYPE-1 (C06-21)

KEK CAMAC STANDARD MODULE (C06-21) C06-21-01
BRANCH TERMINATOR (WITH DISPLAY) KEK TYPE-1

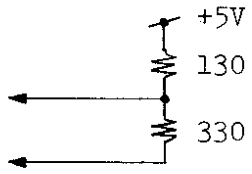
GENERAL

This CAMAC module is designed to terminate the Branch Highway in accordance with EUR 4600e. The module is able to display individual Branch Highway signals in the instantaneous mode (SELF) or the latched mode (BTA). The output from the internal memory unit drive LED display on the front panel to indicate the state of each line of the Branch Highway.

SPECIFICATIONS

(1) Signal standards

All Branch lines are terminated by 93 ohms resistive loads to +5.0V as shown below.

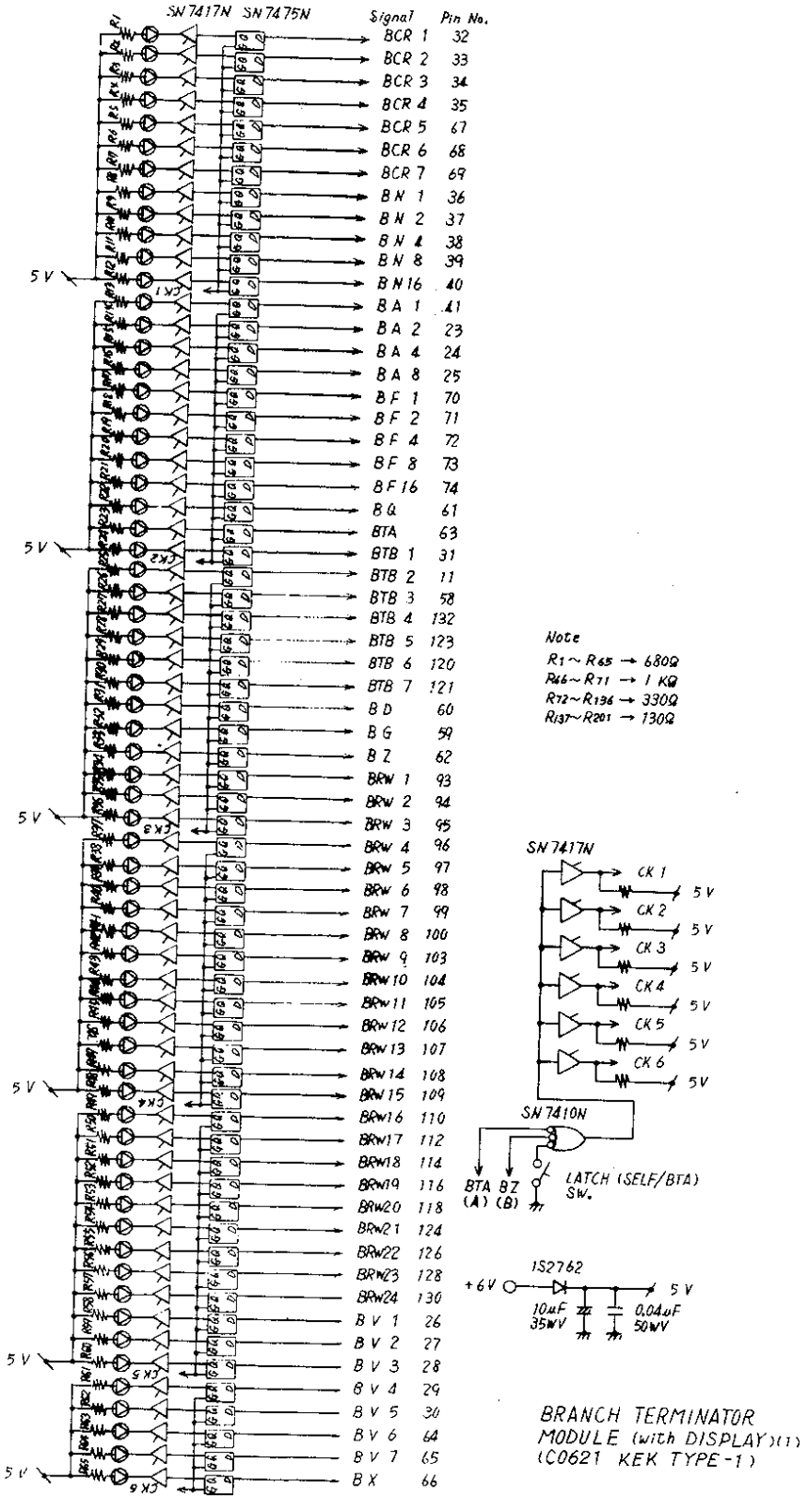


(2) Power requirement

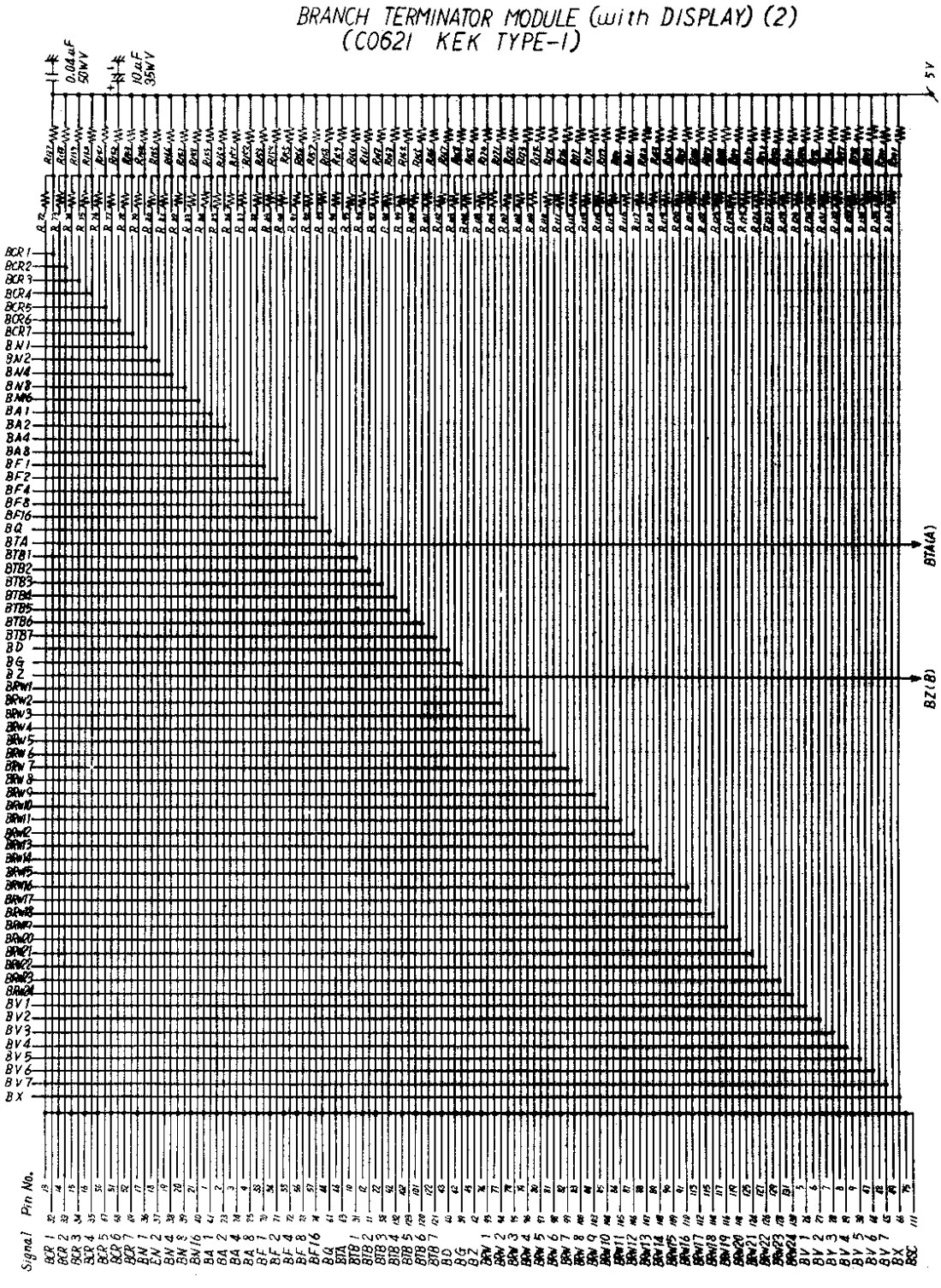
+6V : 800mA (from Right station).
+6V : 820mA (from Left station).

(3) Mechanical

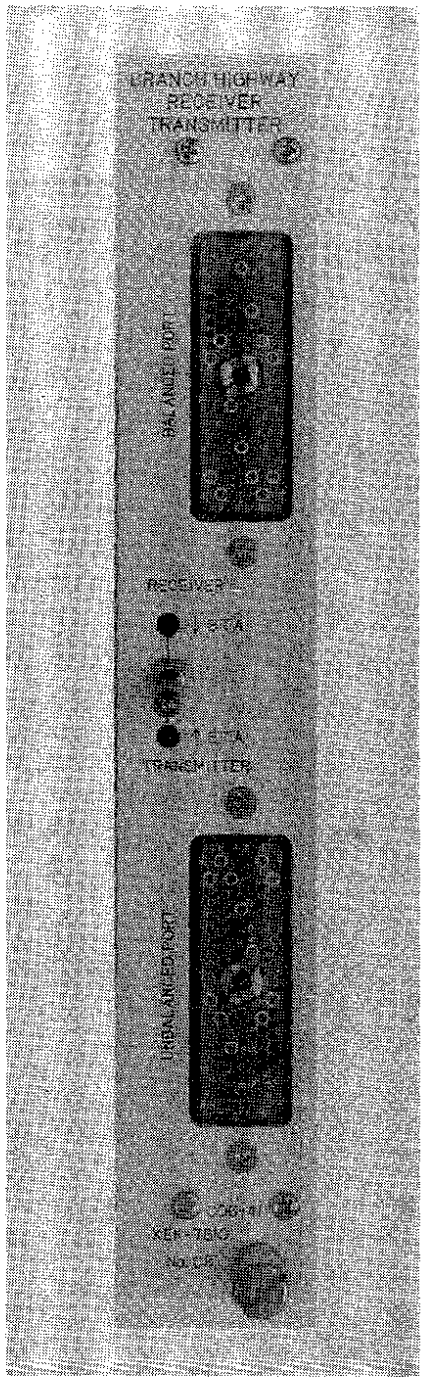
Double-width CAMAC module.
The Branch Highway cable must be connected to the WSS0132-S00-BN000 connector on the front panel.



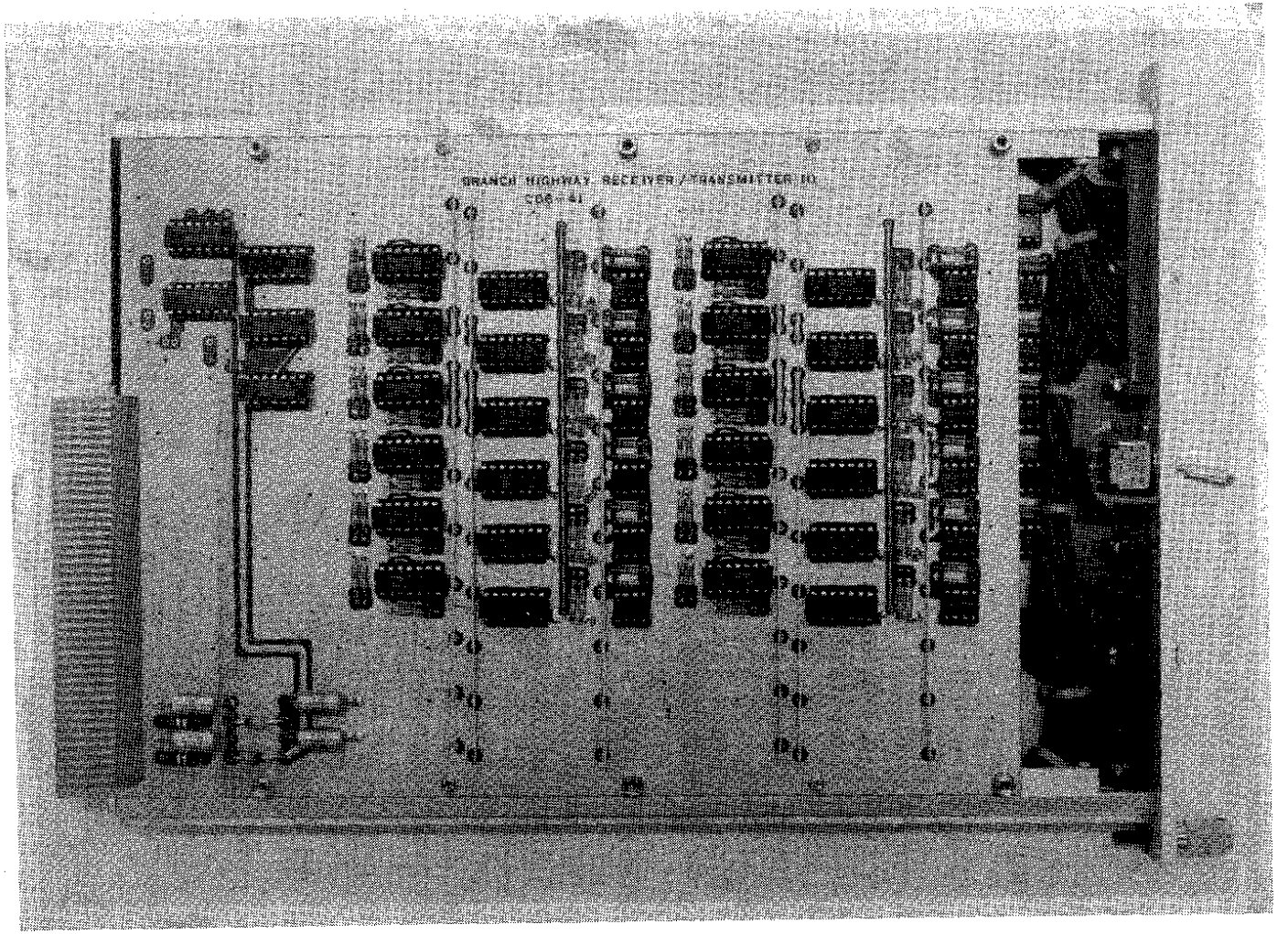
BRANCH TERMINATOR MODULE (with DISPLAY)(1) (C0621 KEK TYPE-1)


BRANCH TERMINATOR MODULE (with DISPLAY) (2)
(C0621 KEK TYPE-I)
0.04 uF 50WV
10 uF 35WV
5V
BTA(A)
BZ(B)
Signal
Pin No.

C06-41 BRANCH HIGHWAY RECEIVER/TRANSMITTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C06-41)
BRANCH HIGHWAY RECEIVER/TRANSMITTER KEK TYPE-1



(INSIDE VIEW)
BRANCH HIGHWAY RECEIVER/TRANSMITTER KEK TYPE-1 (C06-41)

GENERAL

This Branch Highway Tranceiver converts standard CAMAC branch highway signals into balanced signals, or balanced signals into the standard CAMAC branch highway signals. This module allows the extension of a standard CAMAC branch highway over several hundred meters.

OPERATION

There are two modes of operation, transmitting mode and receiving mode, which are selected by the toggle switch in the center of the front panel.

(a) Transmitting mode

When the toggle switch is in the "TRANSMITTER" position, the module works as a transmitter. It must be connected to the branch driver or crate controller near the branch driver. It receives signals BTA, BCR, BN, BA, BF, BZ and BG on standard unbalanced lines and transmits them to another tranceiver used as a receiver in balance signals. On the contrary, signals BTB, BQ, BX and BD are received on balanced lines and transmitted on unbalanced lines. BRW signals are treated according to the direction of the data flow.

(b) Receiving mode

The switch is in the "RECEIVER" position, and the module is in the downstream of the branch highway. The operation in this mode is the reverse of that described above, balanced BTA, BCR, BN, BF and BG are received and converted into unbalance signals and unbalanced BTB, BQ, BX and BD are converted balanced ones. BRW signals are treated also according to the direction of the data flow.

SPECIFICATIONS

(1) Front panel

The front panel include from top to bottom

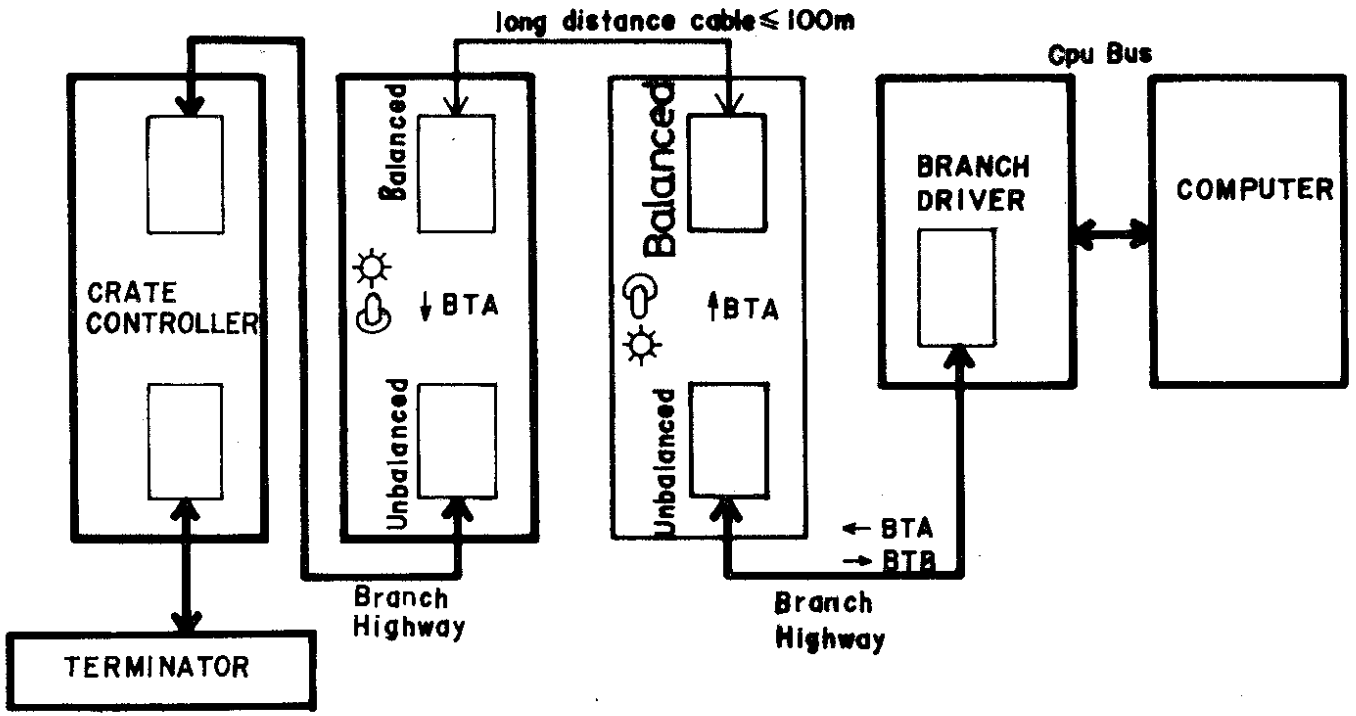
Balanced port : 132-pin Hughes socket connected to balance lines.
Upper LED (↓BTA) : LED is "ON" when the module is in receiving mode.
Toggle switch : Mode selecting switch.
Lower LED (↑BTA) : LED is "ON" when the module is in transmitting mode.
Unbalanced port : 132-pin Hughes socket connected to unbalance lines (Standard CAMAC branch highway).

(2) Power requirement

+6 Volts : 2000 mA.
-6 Volts : 1100 mA.

(3) Mechanical

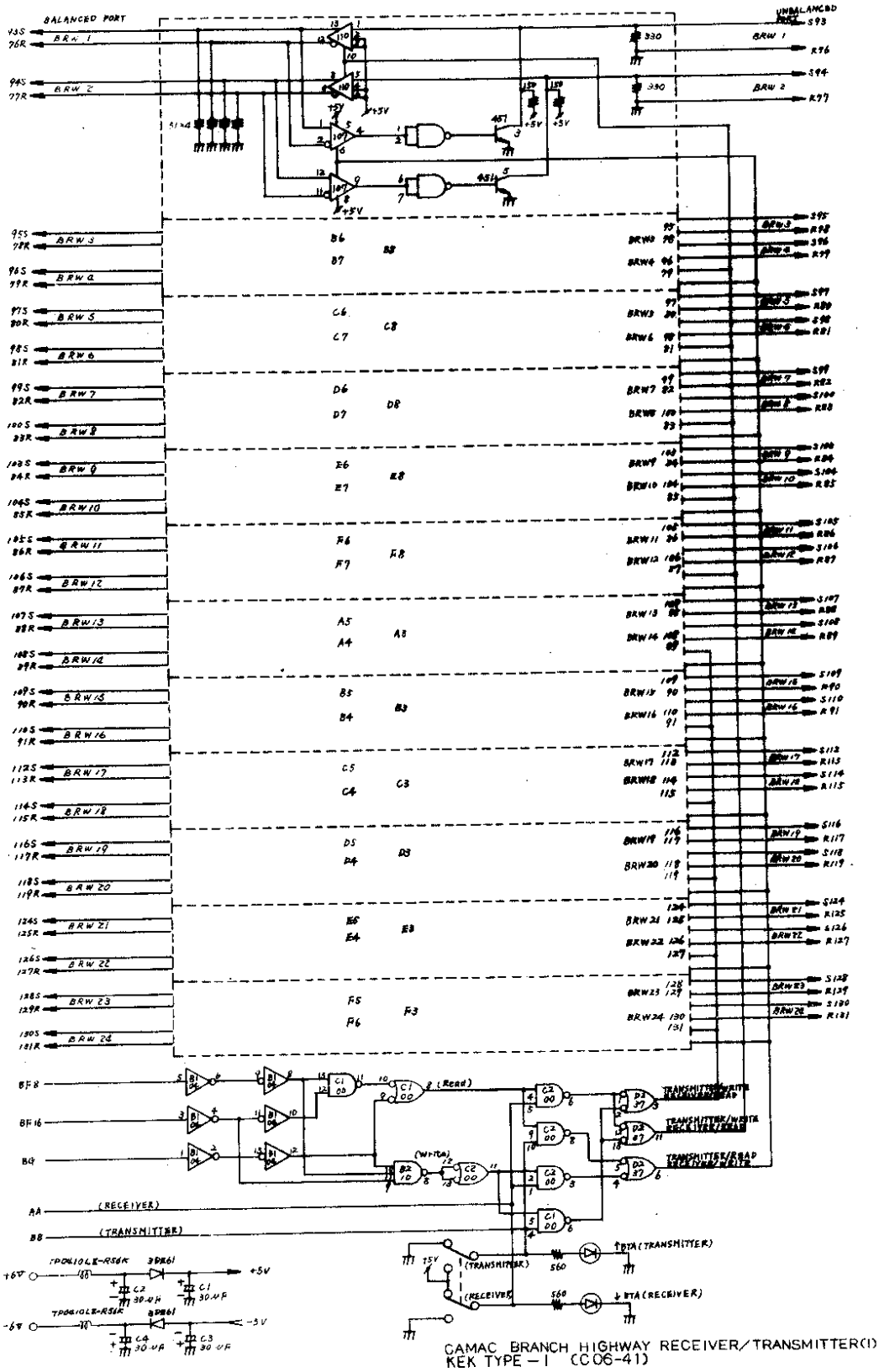
Double width CAMAC standard module.

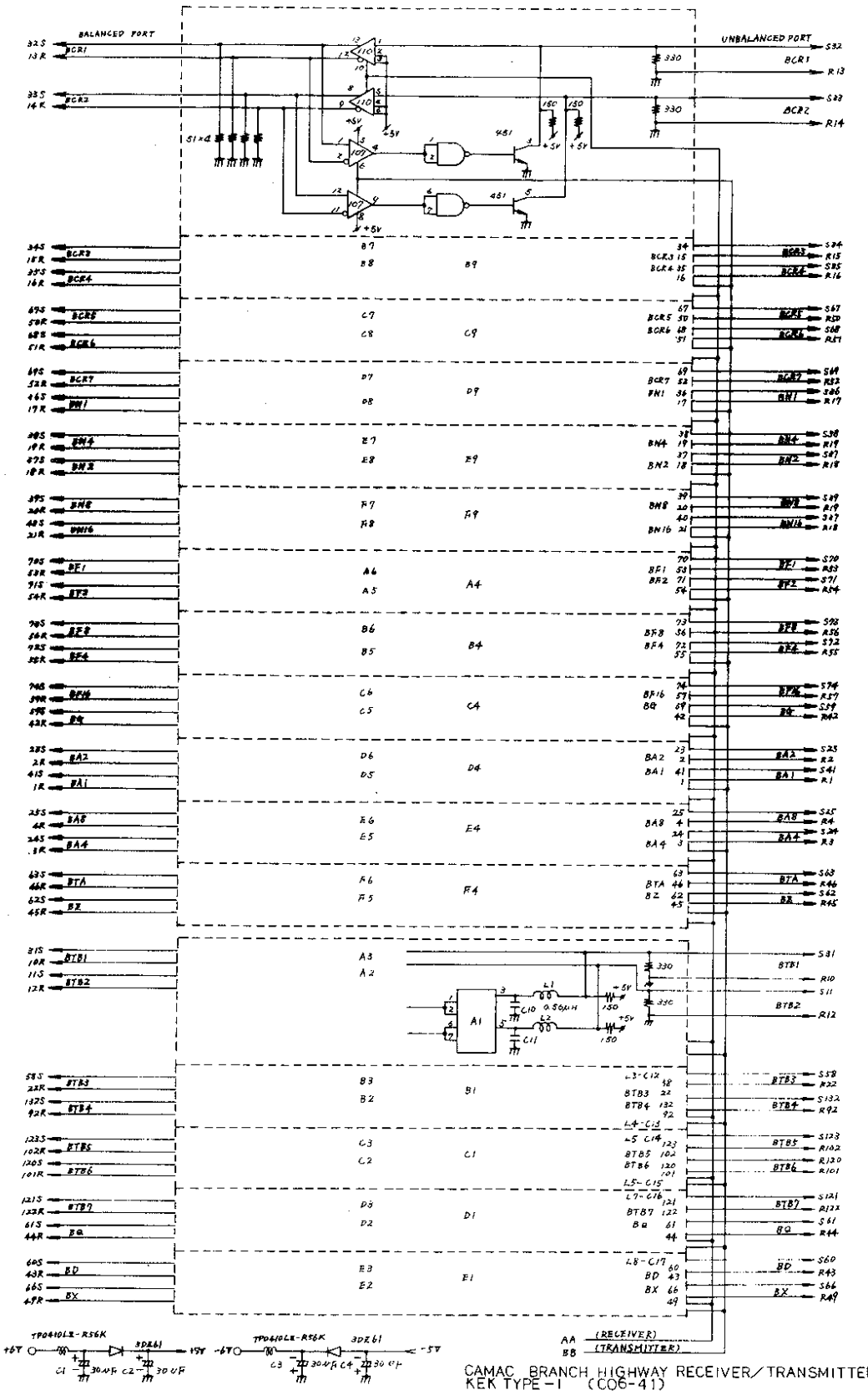


↑BTA (Transmitter)
↓BTA (Receiver)

Read Operation → $\overline{BF8} \cdot \overline{BF16} + \overline{G} = 1$
Write Operation → $\overline{BF8} \cdot BF16 \cdot \overline{G} = 1$

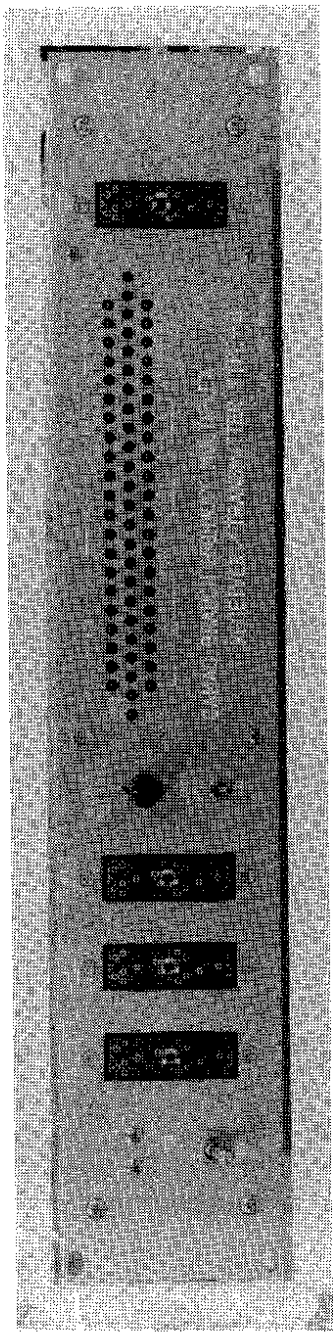
CAMAC BRANCH HIGHWAY
RECEIVER/ TRANSMITTER (C06-41)


BALANCED PORT
UNBALANCED PORT
BRW 1
BRW 2
BRW 3
BRW 4
BRW 5
BRW 6
BRW 7
BRW 8
BRW 9
BRW 10
BRW 11
BRW 12
BRW 13
BRW 14
BRW 15
BRW 16
BRW 17
BRW 18
BRW 19
BRW 20
BRW 21
BRW 22
BRW 23
BRW 24
(RECEIVER)
(TRANSMITTER)
+5V
-5V
CAMAC BRANCH HIGHWAY RECEIVER/TRANSMITTER(I)
KEK TYPE－I (CC06-41)

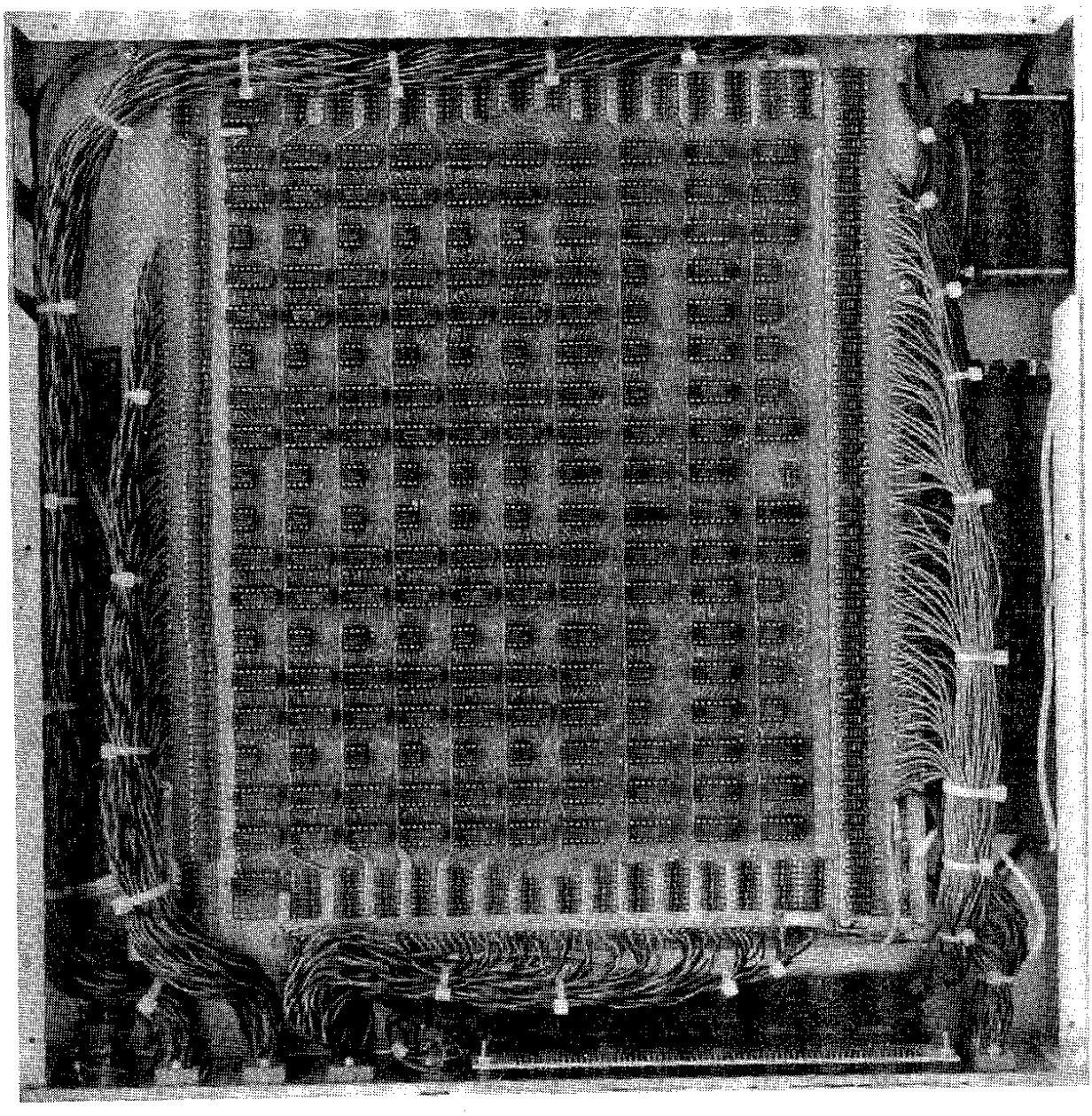


CAMAC BRANCH HIGHWAY RECEIVER/TRANSMITTER(2)
KEK TYPE-1 (C06-41)

C06-42 BRANCH HIGHWAY MULTIPLEX RECEIVER/TRANSMITTER (KEK TYPE-2)



KEK CAMAC STANDARD MODULE (C06-42)
BRANCH HIGHWAY MULTIPLEX RECEIVER/TRANSMITTER
KEK TYPE-2



(INSIDE VIEW)
BRANCH HIGHWAY MULTIPLEX RECEIVER/TRANSMITTER KEK TYPE-2 (C06-42)

KEK CAMAC STANDARD MODULE (C06-42)
BRANCH HIGHWAY MULTIPLEX RECEIVER/TRANSMITTER KEK TYPE-2

GENERAL

This Branch Highway Multiplex Receiver/Transmitter converts standard CAMAC branch highway signals into balanced signals, or balanced signals into standard CAMAC branch highway signals. This module allows the extension of a standard CAMAC branch highway over several hundred meters. This module has one unbalanced port which must be connected to the Branch Driver and three balanced ports connected to the Branch Highway Receiver/Transmitter Module KEK Type-1 (C06-41) used as a receiver. The rotary switch in the center position on the front panel selects one of three balanced ports to be used. The LED on the front panel displays the status of all branch highway signals.

OPERATION

The module works as a transmitter. It receives unbalanced signals BTA, BCR, BN, BA, BF and BZ from the Branch Driver and transfers ones to a balanced port selected by Port Select rotary switch. On the other hand, balanced signals BTB, BQ, BX and BD are transfered to the Branch Driver. BRW signals are treated according to the direction of the data flow.

SPECIFICATIONS

(1) Front panel

Balanced port (1-3) : Three 132-pin Hughes sockets connected to balanced signal lines.
Port select switch (1/2/3) : The rotary switch selects the balanced port channel to be used.
LED Displays : Display the status of all branch highway signals.
Unbalanced port : 132-pin Hughes socket connected to unbalanced signal lines (standard CAMAC branch highway).

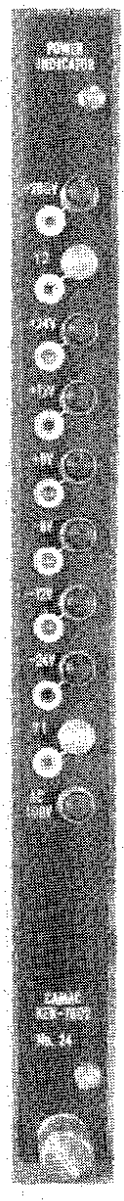
(2) Power supply

This Multiplex Receiver/Transmitter Type-2 contains the power supply in the chassis.

(3) Mechanical

The front panel dimension of this module chassis is 19 inch (482.5 mm) in width and 3-15/32 inch (88 mm) in height.

C07-11 POWER INDICATOR (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C07-11)
POWER INDICATOR KEK TYPE-1

KEK CAMAC STANDARD MODULE (C07-11)
POWER INDICATOR KEK TYPE-1

GENERAL

This Power Indicator module provides visual indication of all the power supplies present on the dataway of a CAMAC crate. With the exception of the AC 100 V power line, a monitor terminal is provided for each line.

This module can be inserted in any normal CAMAC crate position.

SPECIFICATIONS

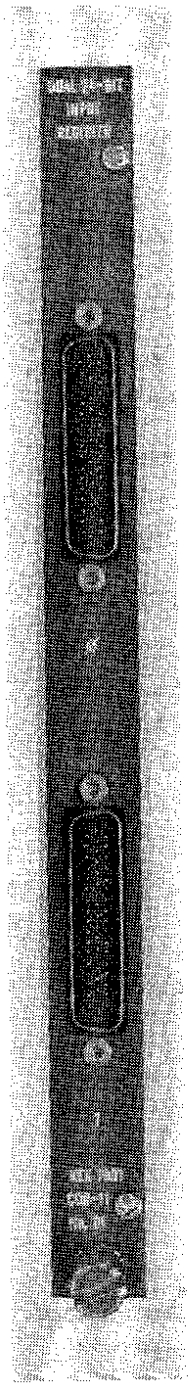
(1) Packaging : Single width CAMAC standard module. Conforms to ESONE Report EUR 4100e standards.

(2) Power requirements : All LED lamps +24V, +12V, +6V, -6V, -12V, -24V, demand 50 mA.
Neon lamps +200V, AC 100V demand 0.5 mA.

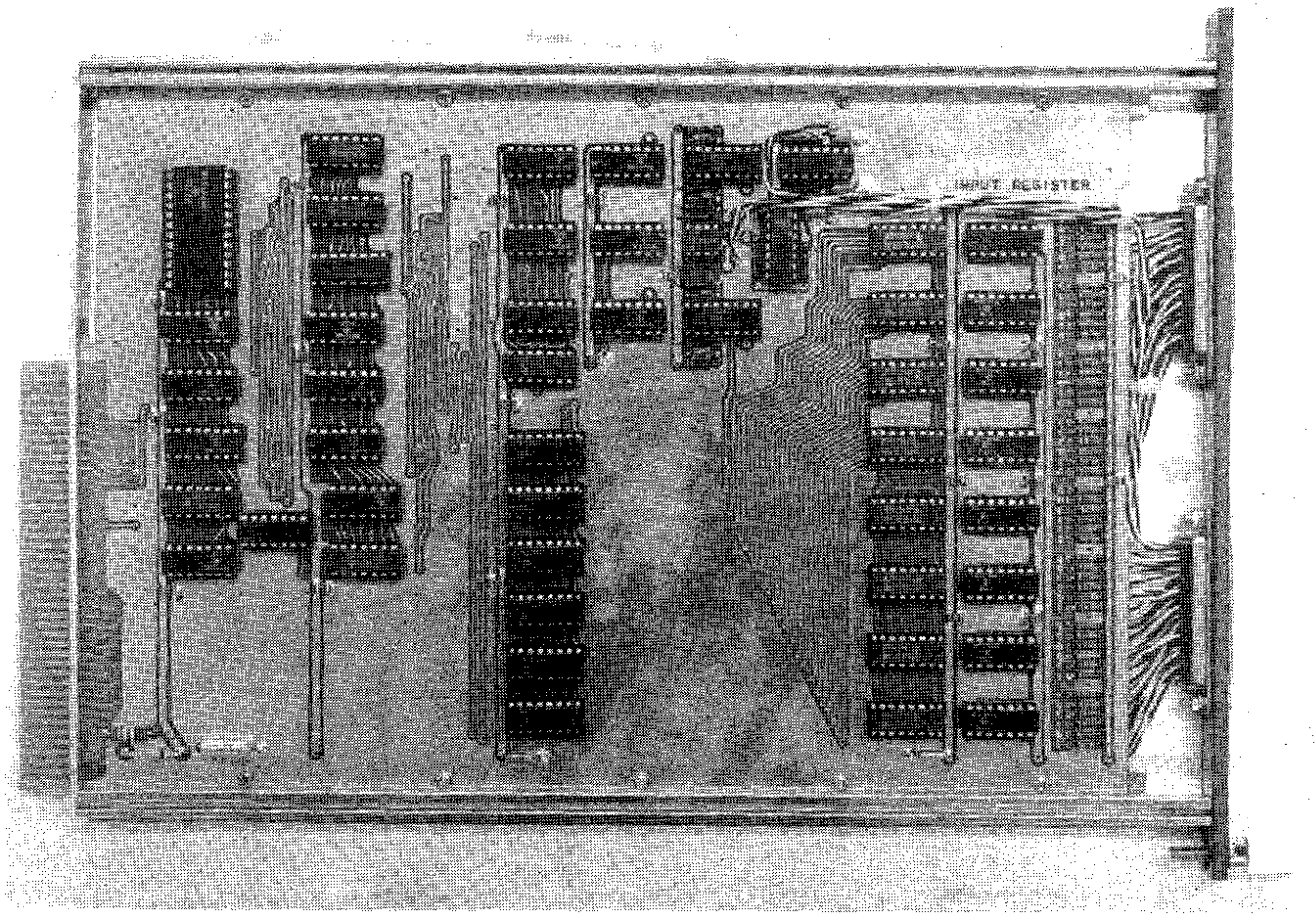
(3) Use of dataway : Access of all power lines only.

(4) Indicators : Low voltage level indicators are the LED type. High voltage level indicators are the neon lamp type.

C08-11 DUAL 24-BIT INPUT REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-11)
DUAL 24-BIT INPUT REGISTER KEK TYPE-1



(INSIDE VIEW)
DUAL 24-BIT INPUT REGISTER KEK TYPE-1 (C08-11)

KEK CAMAC STANDARD MODULE (C08-11) C08-11-01
DUAL 24-BIT INPUT REGISTER

GENERAL

The C08-11 Input Register was designed to receive 24-bit digital data in parallel negative true TTL logic form. The specifications are almost the same as these of the RI224, Input Register of ORTEC, except that the Cannon connectors 2DB52S on the front panel are replaced by the one 2DB52P in order to make KEK standard Cannon cables be utilized.

SPECIFICATIONS

(1) Functions

F(0)A(K) : Read Register K (K=0, 1). Returns X, Q.
F(2)A(K) : Read and Clear Register K (K=0, 1). Returns X, Q.
F(1)A(12) : Read LAM Status Register. Returns X, Q.
F(1)A(13) : Read LAM Mask Register. Returns X, Q.
F(8)A(0) : Test LAM. Returns X. Returns Q only if LAM 0 or LAM 1 is true. The LAM signal cannot be generated during the presence of the Dataway N signal.
F(10)A(K) : Clear LAM K (K=0,1). Returns X, Q.
F(17)A(13) : Write LAM Mask Register. Returns X, Q.
F(28)A(K) : Load Register K (K=0, 1). Returns X, Q.
(C+Z)S2 : Reset both data registers to 0 and all control and status flip-flops to their respective initial conditions.
I : Inhibit generation of load pulse signals.

(2) Front panel

24-bit data and three control signals are fed into the module through two Cannon 2DB52P 52pin connectors on the front panel The pin assignment is given in table 1.

(3) Power requirement

+6V : 470mA

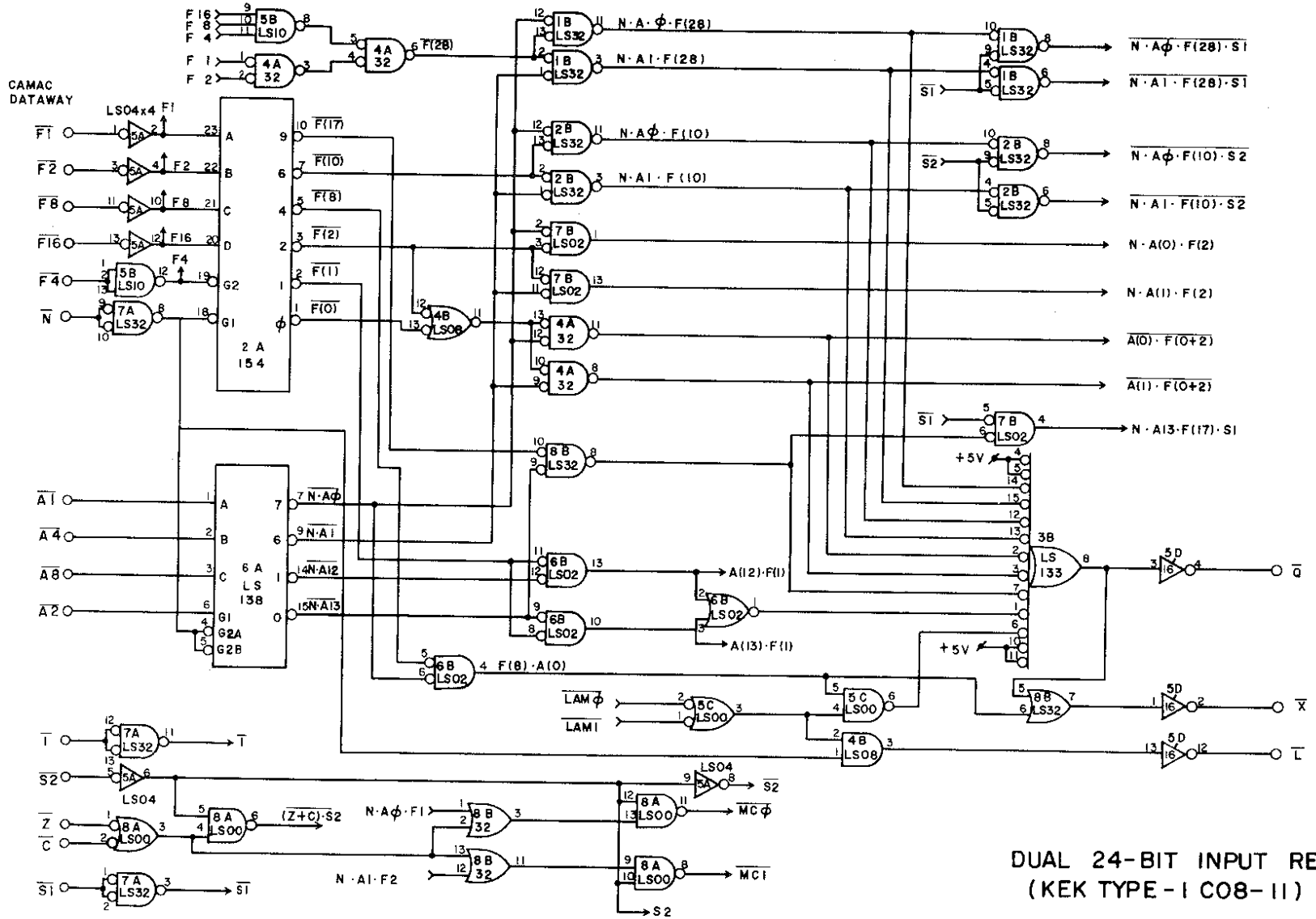
(4) Mechanical

Single width CAMAC standard module.

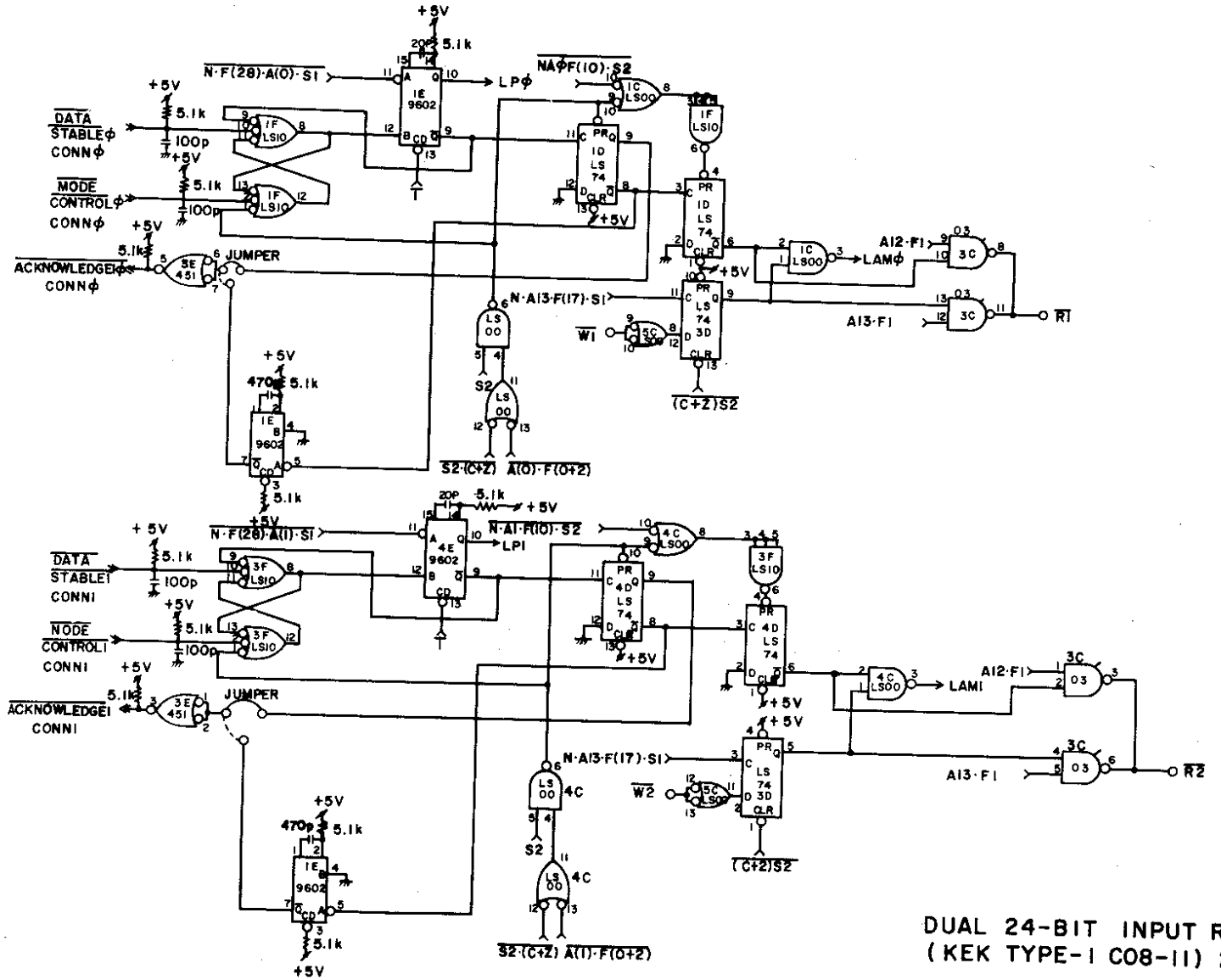
Data or Control Bit	Pin Number	
	Signal	Return*
R1	17	16
R2	35	34
R3	51	52
R4	15	14
R5	33	32
R6	49	50
R7	13	12
R8	31	30
R9	45	46
R10	29	28
R11	11	10
R12	47	48
R13	9	8
R14	27	26
R15	43	44
R16	7	6
R17	23	22
R18	5	4
R19	41	42
R20	25	24
R21	39	40
R22	3	2
R23	21	20
R24	37	38
Mode Control 0 or 1	1	18
Data Stable 0 or 1	19	18
Data Acknowledge 0 or 1	36	18

* All signal return pins on front panel connectors 0 and 1 are connected to module chassis ground.

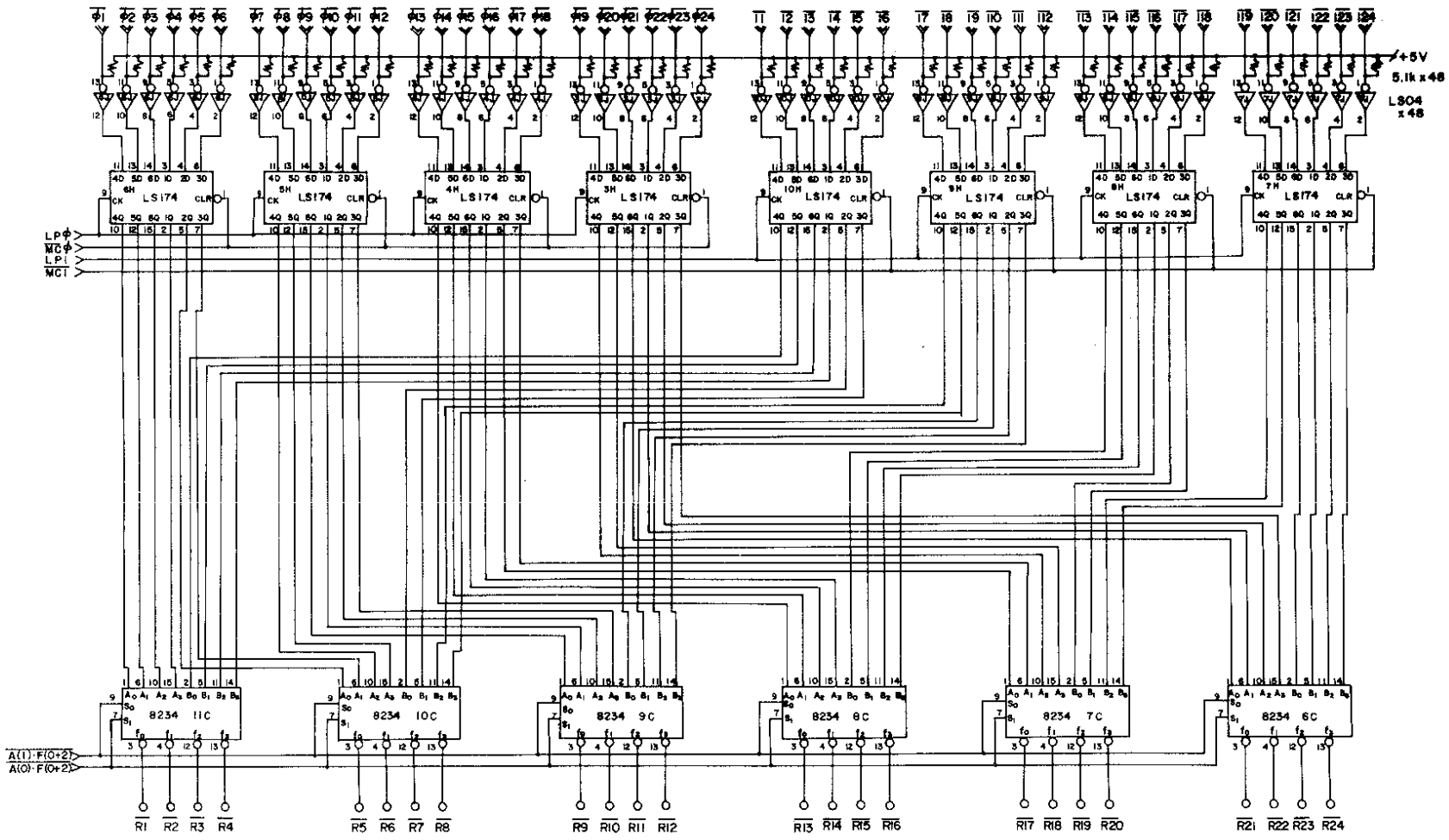
Table 1. Front Panel Connector Pin Assignments.

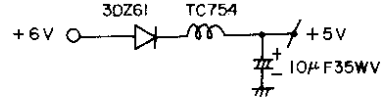


DUAL 24-BIT INPUT REGISTER
(KEK TYPE-1 C08-11) 1/3



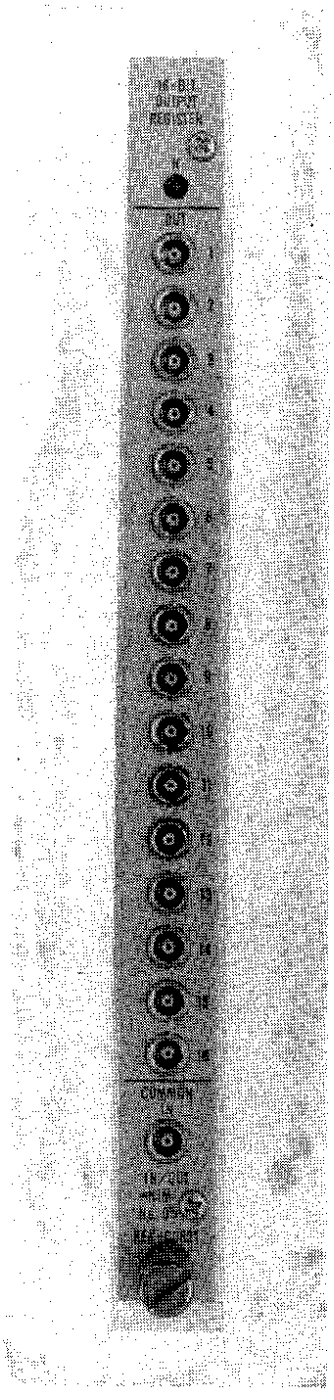
DUAL 24-BIT INPUT REGISTER
(KEK TYPE-I C08-11) 2/3



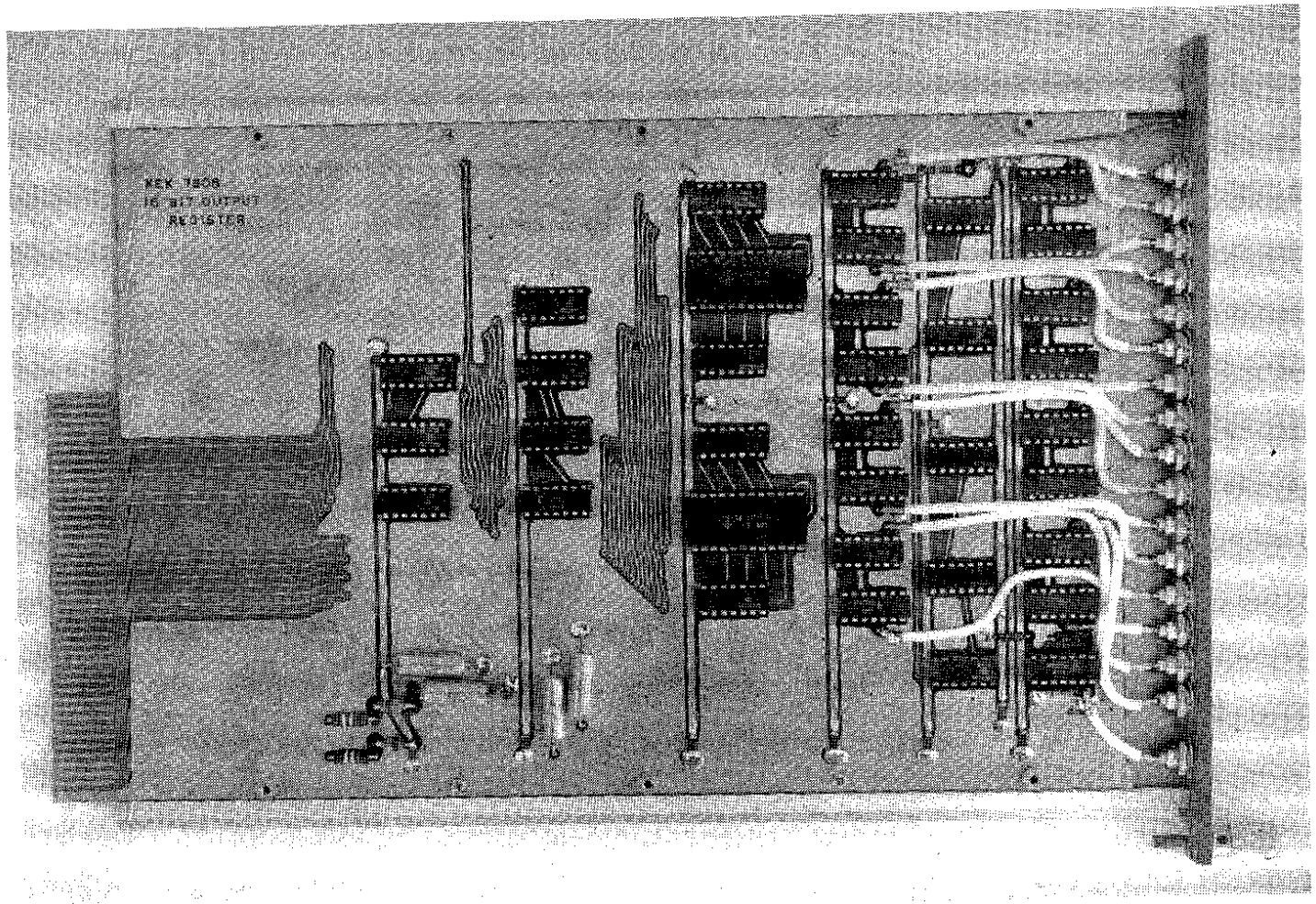


DUAL 24-BIT INPUT REGESTER
(KEK TYPE-I C08-11) 3/3

C08-21 16-BIT OUTPUT REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-21)
16-BIT OUTPUT REGISTER KEK TYPE-1



(Inside View)
16-BIT OUTPUT REGISTER KEK TYPE-1 (C08-21)

KEK CAMAC STANDARD MODULE (C08-21)
16-BIT OUTPUT REGISTER KEK TYPE-1

GENERAL

This module provides 16 NIM logic signals in the level or the pulse mode. The 16-bit word is written out from the computer by a CAMAC function. These 16 signals are used as control signals for the external equipment, or as an event simulation for the automatic test of the experimental set up.

At the same time this module works as a fan out of a NIM logic signal when applied to the front panel connector COMMON IN. Therefore, the output pulses are OR'ed signals of this NIM input pulse and the 16-bit word written from the computer.

SPECIFICATIONS

(1) CAMAC function

F(9)A(0)S2 : Clear 16-bit register.
F(16)A(0)S1 : Write a 16-bit word into the register. This function produces level output.
F(17)A(0)S1 : Write a 16-bit word to the register which generates pulse output with the duation from S1 to S2.
(Z+C)S2 : Clear 16-bit register.
Q : Generate Q(Q=1) for F(16)A(0), and F(17)A(0).

(2) Front panel

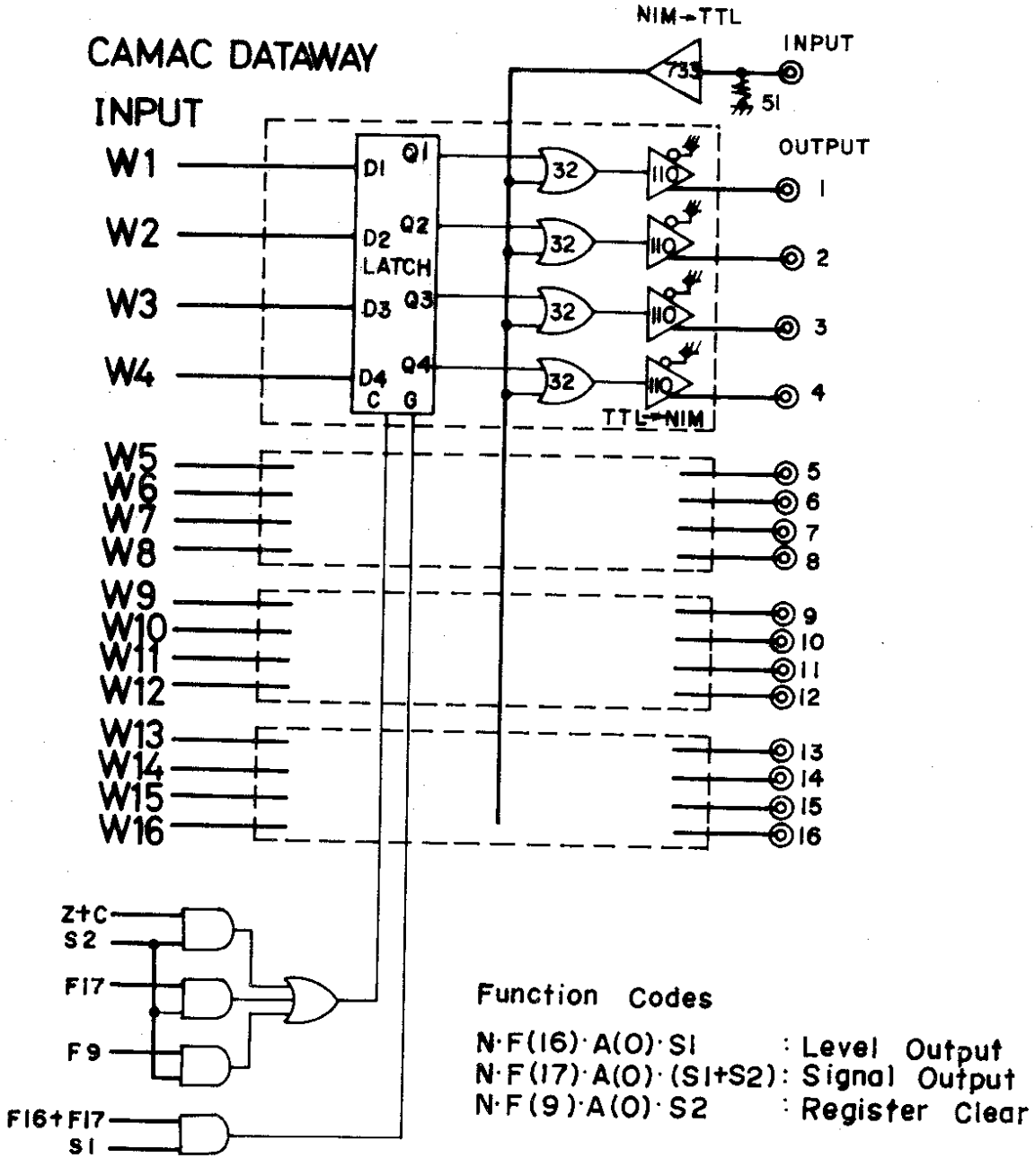
OUTPUT 1-16 : (LEMO RA00250) NIM fast logic signals, 50 ohms.
COMMON IN : (LEMO RA00) NIM fast logic signal, 50 ohms. Input signal for the Fan out.

(3) Power requirement

+6 Volts : 710 mA.
-6 Volts : 340 mA.

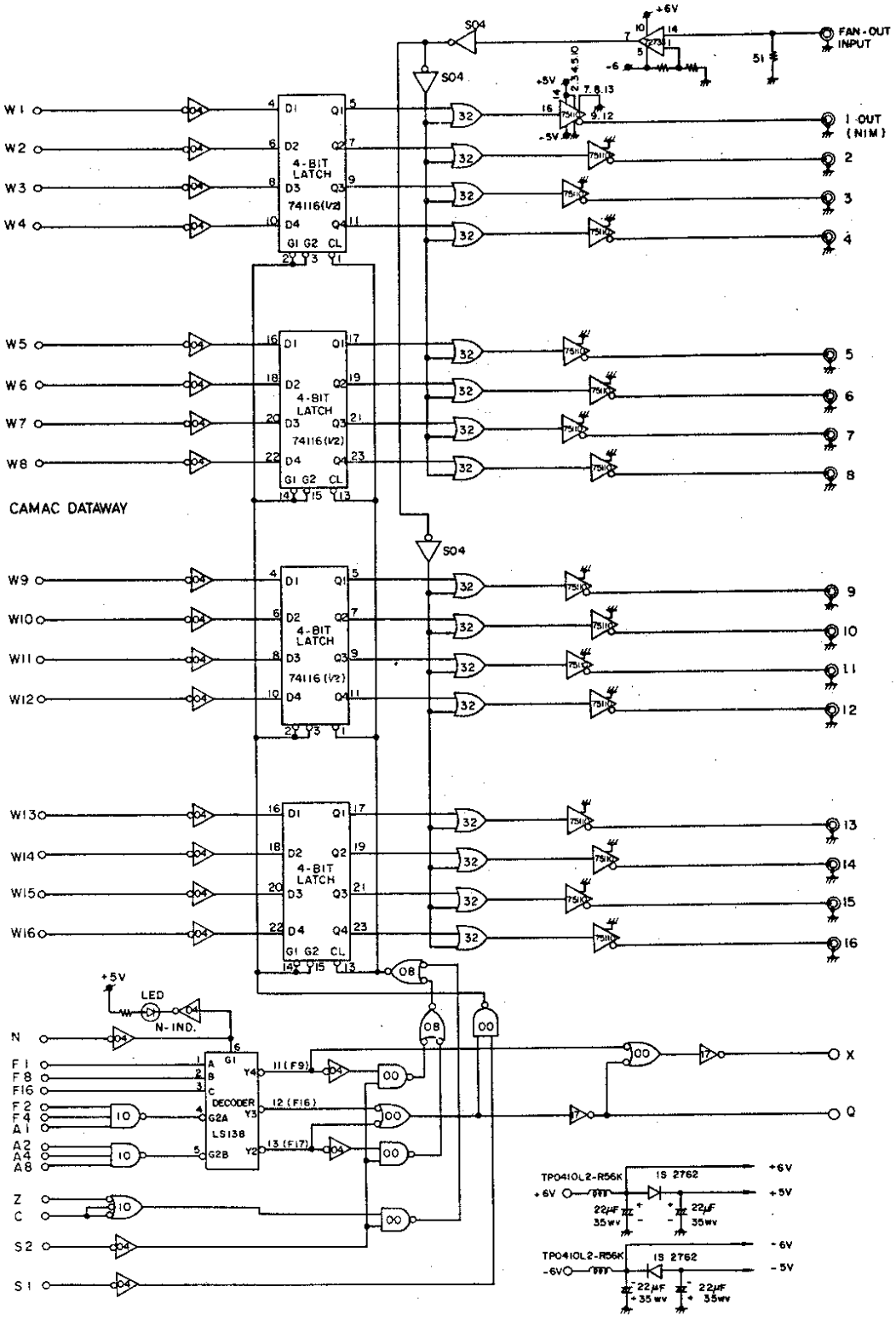
(4) Mechanical

Single width CAMAC standard module.



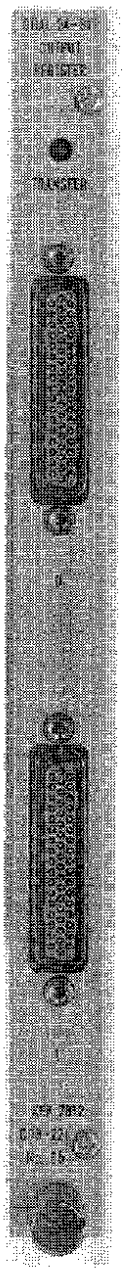
16-BIT OUTPUT REGISTER BLOCK DIAGRAM

(C08-21 KEK TYPE-1)

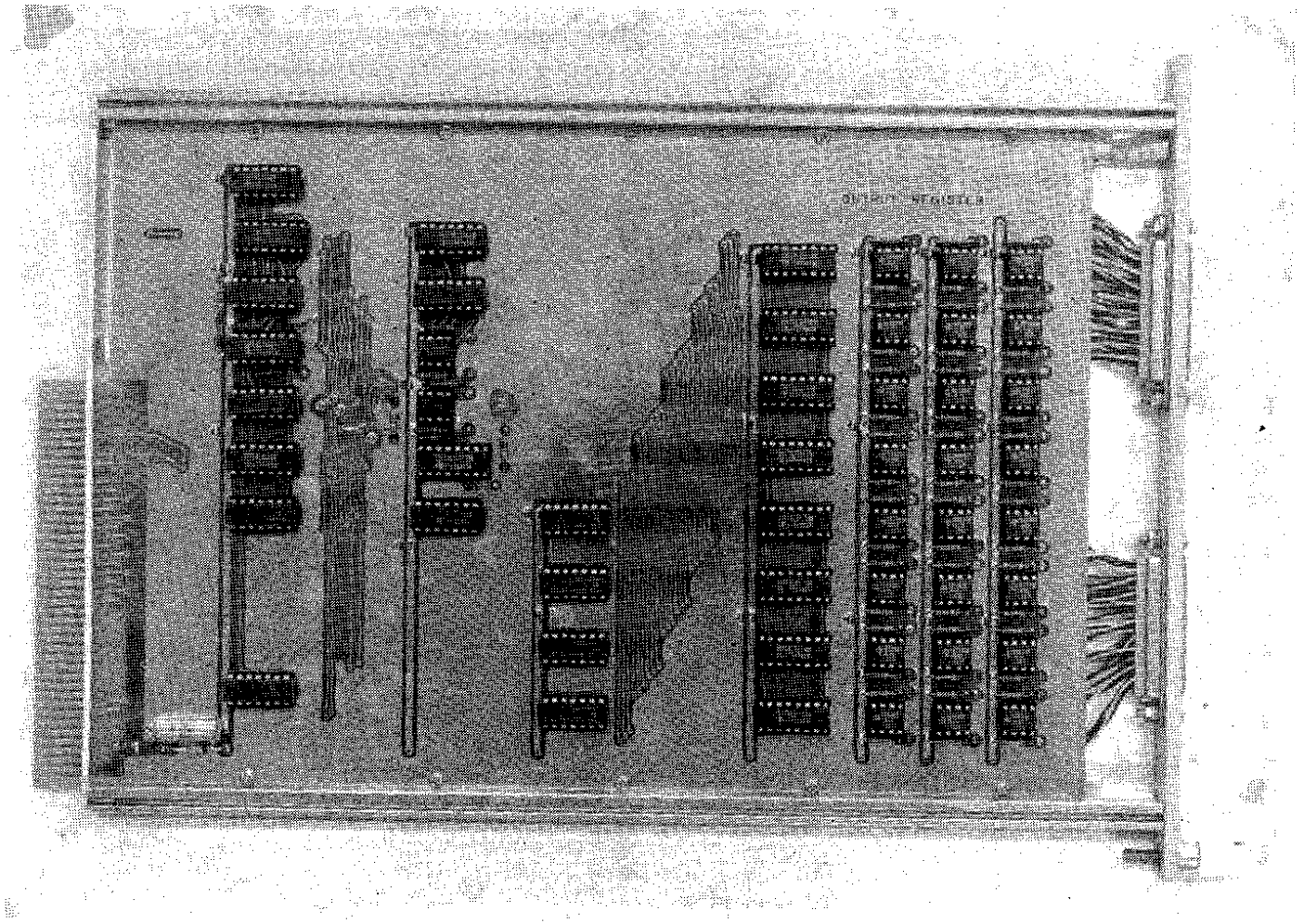


16-BIT OUTPUT REGISTER
(C08-21 KEK TYPE-1)

C08-22 DUAL 24-BIT OUTPUT REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-22)
DUAL 24-BIT OUTPUT REGISTER KEK TYPE-1



(INSIDE VIEW)
DUAL 24-BIT OUTPUT REGISTER KEK TYPE-1(C08-22)

KEK CAMAC STANDARD MODULE (C08-22) C08-22-01
DUAL 24-BIT OUTPUT REGISTER

GENERAL

The C08-22 Output register is dual 24-bit register which transfer the output data in parallel negative true TTL logic form. The specifications are almost the same as these of the R0244 Output Register of ORTEC.

SPECIFICATIONS

(1) Functions

F(1)A(0) : Reads Status. Returns X, Q. Status assignment is given in table 1.
F(16)A(k) : Write data into storage register and generate control signals on the output dataway.
C S2 : Resets both storage registers to 0.
Z S2 : Resets both storage registers and all status registers and control flip-flops to 0.

(2) Front panel

24-bit data and three control signals are fed out or into the module through two Cannon 2DB52P 52-pin connectors on the front panel. The pin assignment is given in table 2.

LED on the top of the front panel shows that the response is not returned from the external device.

(3) Power requirement

+6V : 420mA

(4) Mechanical

Single width CAMAC standard module.

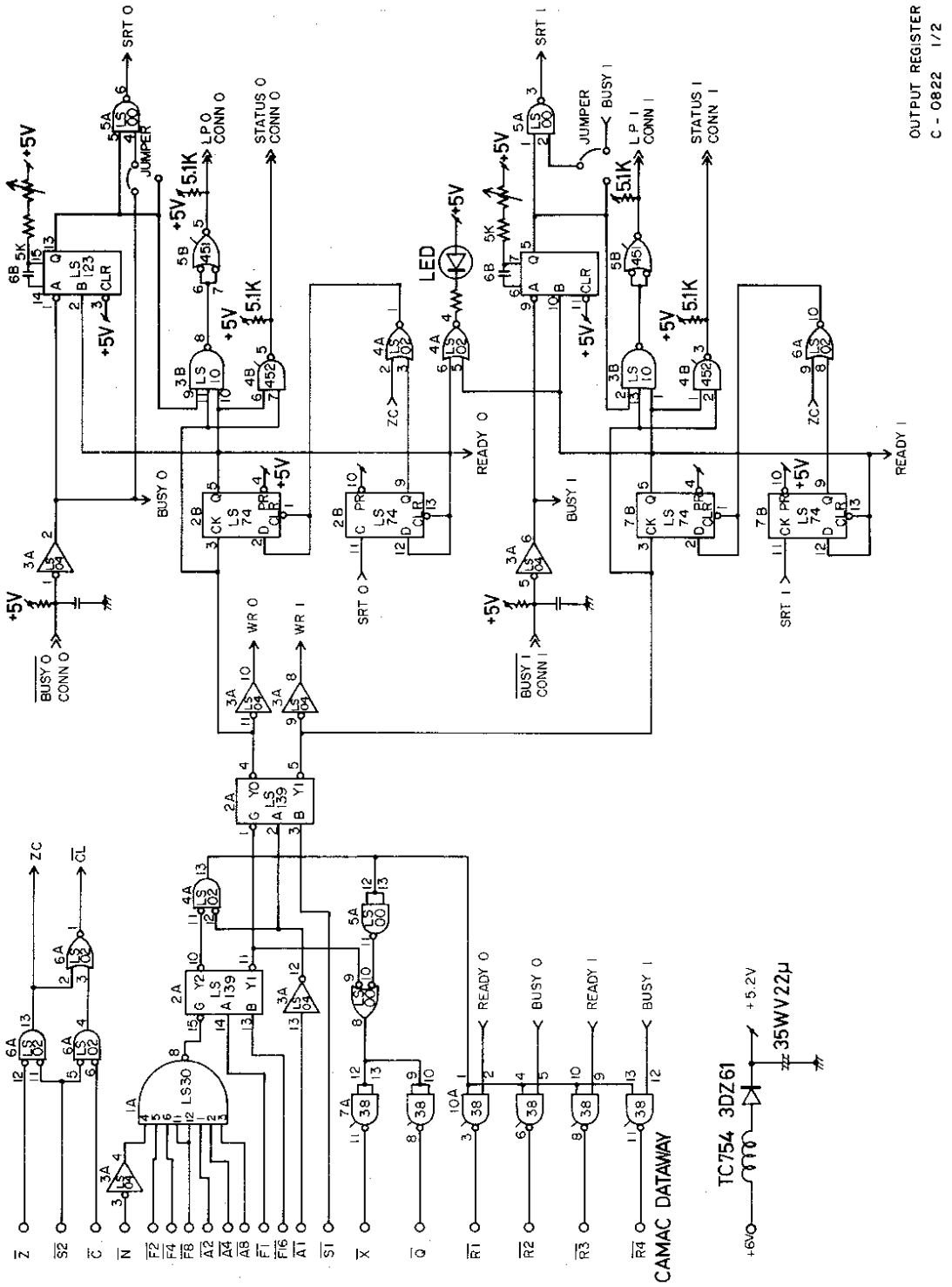
bit	status
R1	Data Ready 0
R2	Busy 0
R3	Data Ready 1
R4	Busy 1

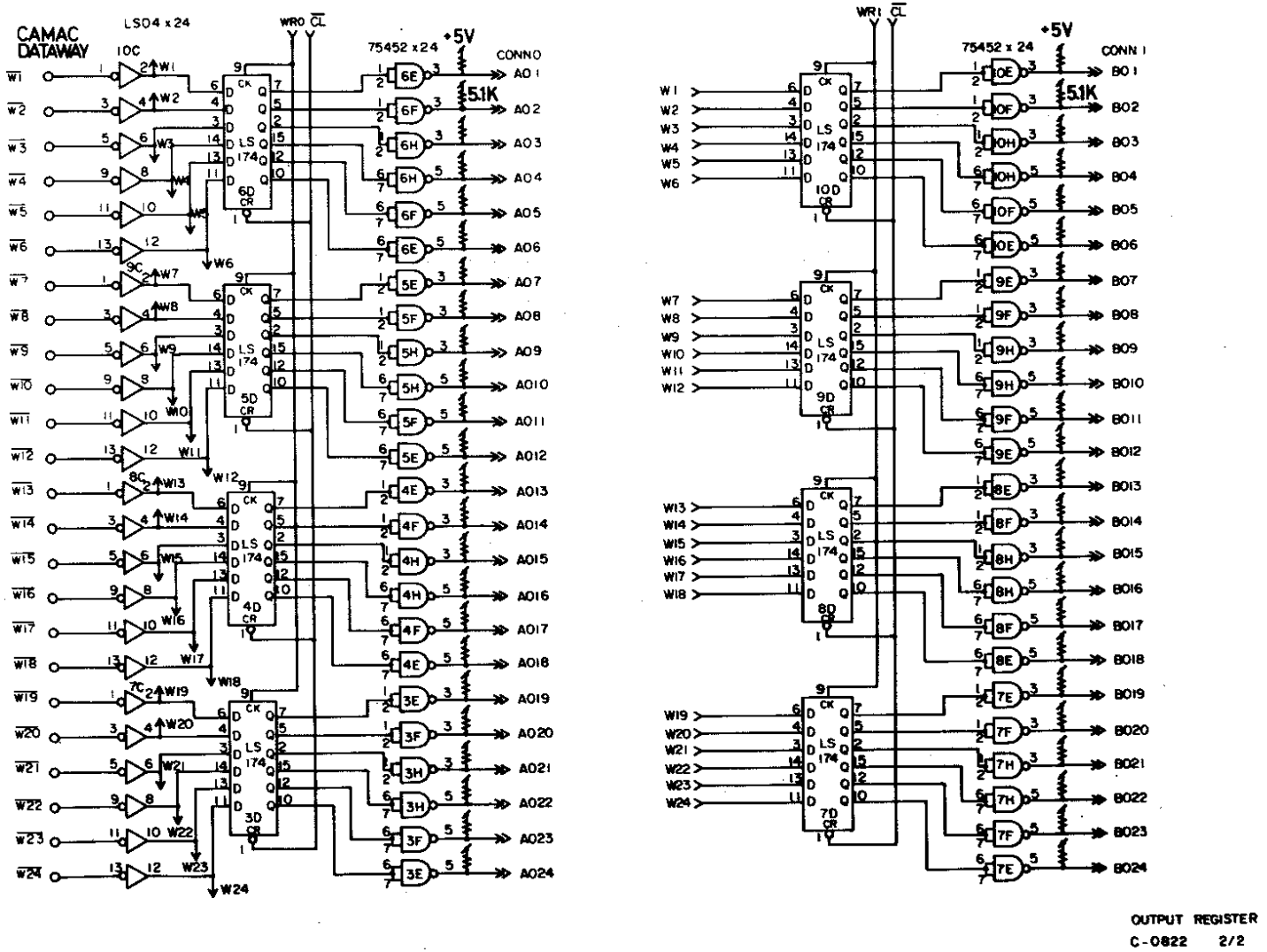
Table 1. Status bit assignment

Data or Control Bit	Pin Number	
	Signal	Return*
W1	17	16
W2	35	34
W3	51	52
W4	15	14
W5	33	32
W6	49	50
W7	13	12
W8	31	30
W9	45	46
W10	29	28
W11	11	10
W12	47	48
W13	9	8
W14	27	26
W15	43	44
W16	7	6
W17	23	22
W18	5	4
W19	41	42
W20	25	24
W21	39	40
W22	3	2
W23	21	20
W24	37	38
Status 0 or 1	1	18
Load Pulse 0 or 1	19	18
Busy 0 or 1	36	18

* All signal return pins on front panel connectors 0 and 1 are connected to module chassis ground.

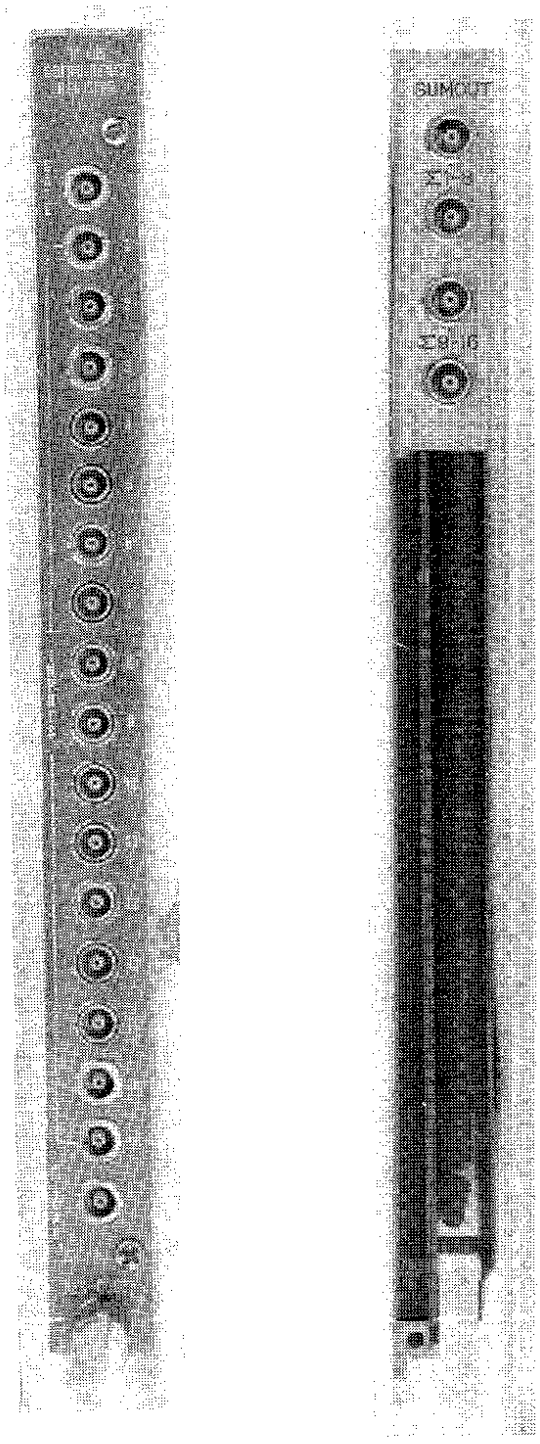
Table 2. Front Panel Connector Pin Assignments.


OUTPUT REGISTER
C - 0822 1/2
CAMAC DATAWAY
TC754 3DZ61
35WV22µ
+5.2V
+6V
LED
JUMPER
SRT O
SRT I
LP O
CONN O
LP I
CONN I
STATUS O
CONN O
STATUS I
CONN I
BUSY O
BUSY I
READY O
READY I
WR O
WR I
ZC
CL
LS30
LS 74
LS 139
5.1K
5K

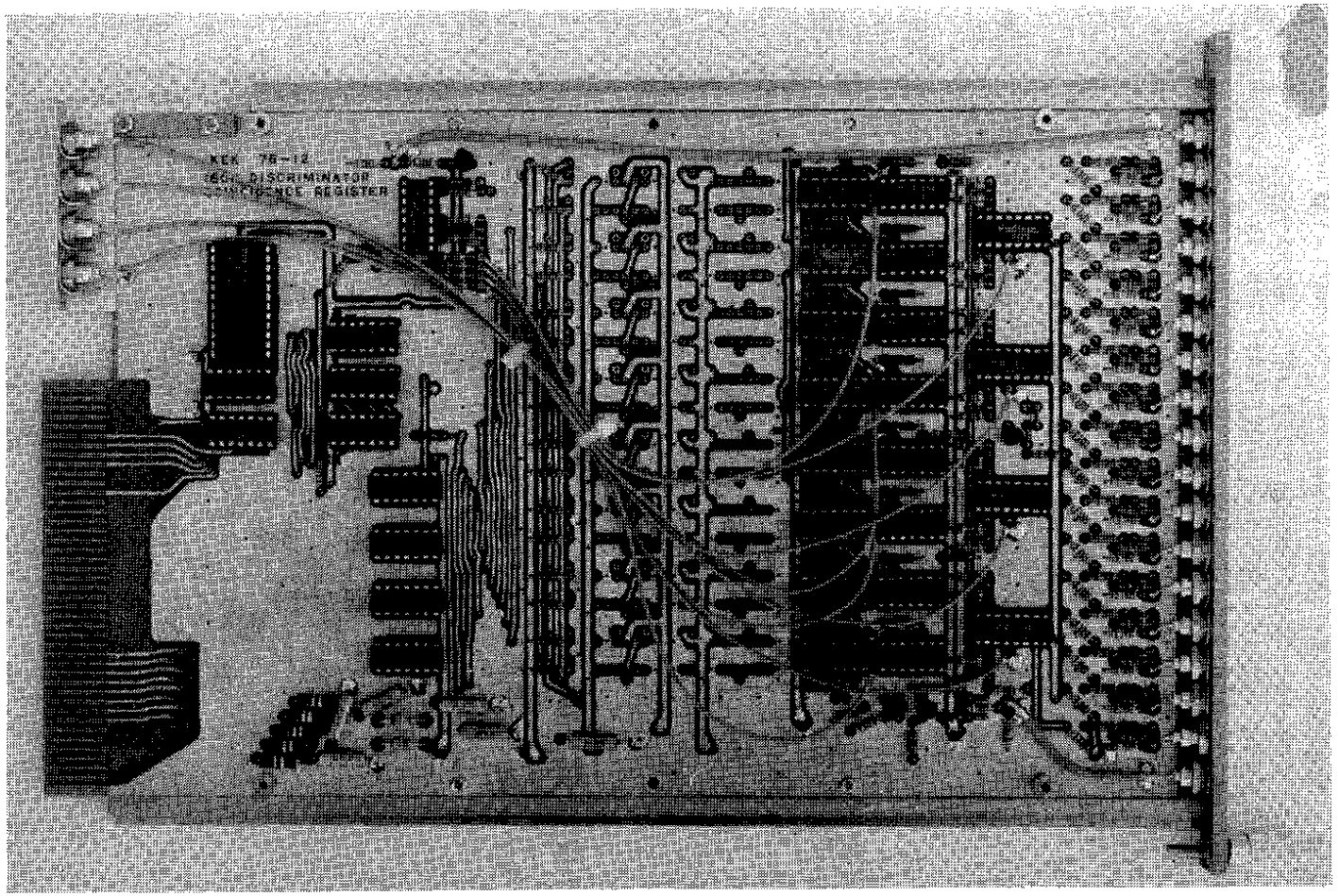


OUTPUT REGISTER
C-0822 2/2

C08-31 16-CH COINCIDENCE REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (Co8-31)
16-CH COINCIDENCE REGISTER KEK TYPE-1



(Inside View)
16-CH COINCIDENCE REGISTER KEK TYPE-1 (C08-31)

KEK CAMAC STANDARD MODULE (C08-31) C08-31-01
16-CHANNEL COINCIDENCE REGISTER KEK TYPE-1

GENERAL

This Coincidence Register operates from standard NIM fast logic levels. The logic channels, which seek a coincidence between each input and a common fast gate input, employ MECL 10K integrated circuits and provide coincidence resolving times under 2 nsec. Logical "1" data levels, representing the time coincidence between the common fast gate and the 16 inputs, are stored in a 16-bit fast buffer register for later readout under CAMAC commands.

SPECIFICATIONS

(1) Input characteristics

Inputs : 16, Lemo connectors; impedance 50 ohms ±5%; direct-coupled; protected to ±10 volts for inputs <1 μs; reflections <10% for 2 ns risetime.

Input Threshold : Accepts standard AEC/NIM fast logic levels (-500 mV nominal).

Double Pulse Resolution : 10 ns max.; 8 ns typical.

Gate Input : One, Lemo connector; 50 ohms impedance; -600 mV or greater enables; minimum duration at full logic level (-750 mV) 2.0 ns; protected to ±100V. Should precede inputs by at least 4 ns.

Clear Input : One, Lemo connector: -600 mV or greater, 50 ohms impedance; minimum duration 10 ns; protected ±100V. 10 ns settling time after clear.

(2) Output characteristics

Data Readout : CAMAC function and address commands gate the 16 binary bits on to the 2^0 to 2^{15} CAMAC dataway bus lines; logical 1, ≤0.5 volts (0 to 16 mA); logical 0, open circuit (≤100 μA at 5.5 volts).

Summing Outputs : 2; one pair of high impedance bridged connectors for each set of 8 inputs; 4 mA ±3% is presented for each register latched; maximum output into 25 ohms, -1 volt for single or cascaded units (corresponds to 10 set registers); risetime, 4 ns (increasing slightly for multiple levels); delay of leading edge of summing output from leading edge of input, 20 ns.

(3) General

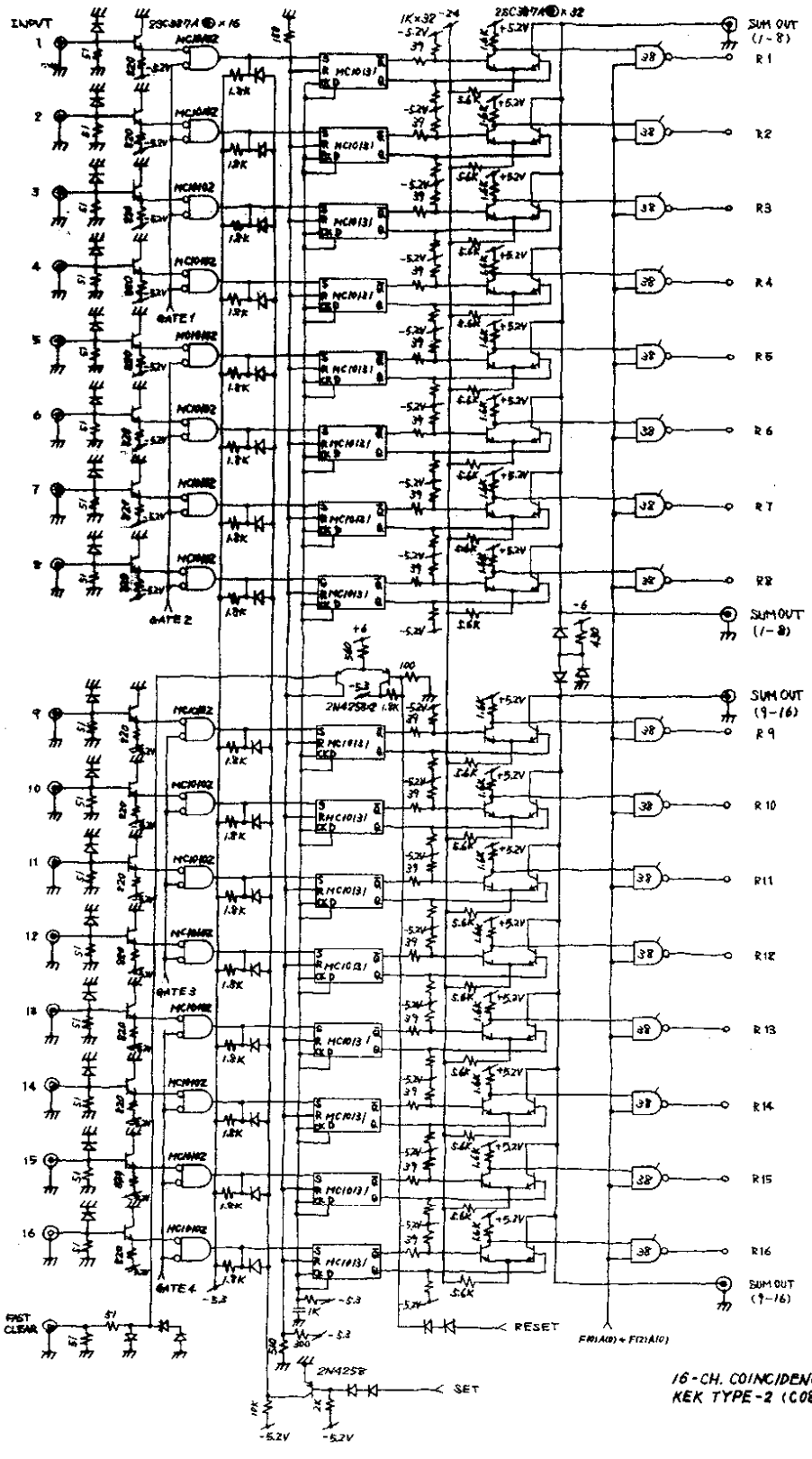
Coincidence Width : 1 ns up, determined by input and gate pulse durations.

CAMAC Commands : Z or C: Clears register, requires S2.
I: Gate Input is inhibited for duration of CAMAC inhibit commands.
Q: Q=1 response is generated in recognition of an F(0), F(9) or F(25) for a valid N and A(0), but there will be no response (Q=0) under any other condition.
X: X=1 (Command Accepted) response is generated when a valid F, N and A command is generated.

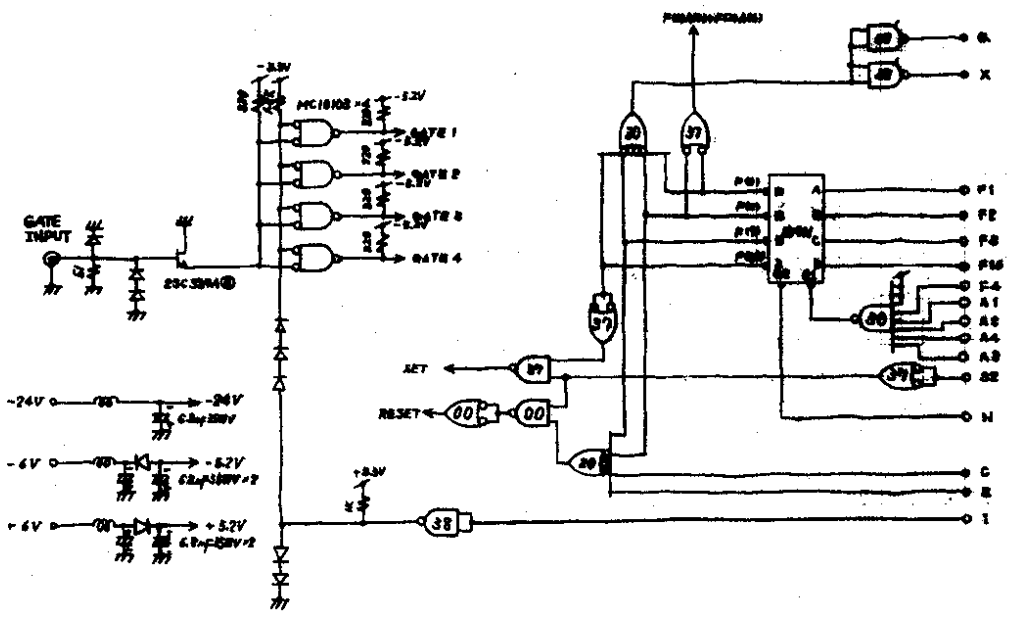
CAMAC Function Codes : F(0): Read group 1 register; requires N and A(0).
F(2): Read and Clear group 1 register; requires N, A(0) and S2.
F(9): Clear Group 1 register; requires N, A(0) and S2.
F(25): Increment (test mode latches all channels); requires N and S2.

Pachaging : CAMAC single-width module. Conforms to ESONE Report EUR 4100e standards.

Power Requirements : +6 Volts at 140 mA;
-6 Volts at 640 mA;
-24 Volts at 64 mA.

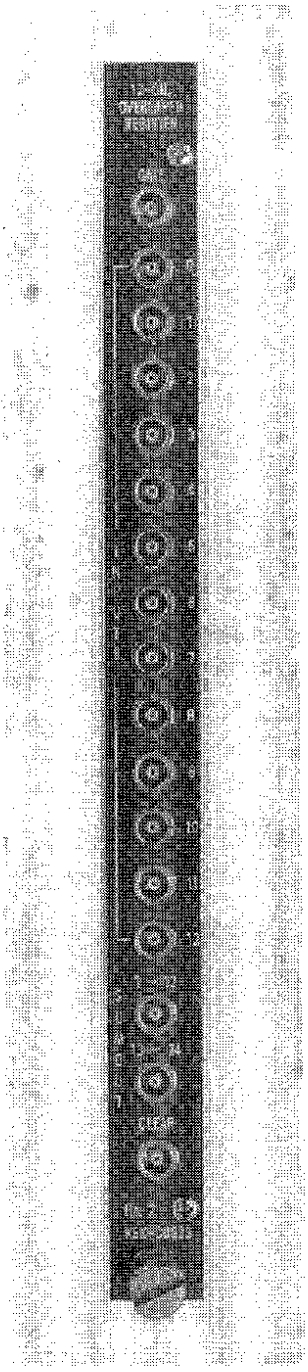


16-CH. COINCIDENCE REGISTER (1)
KEK TYPE-2 (C08-31)

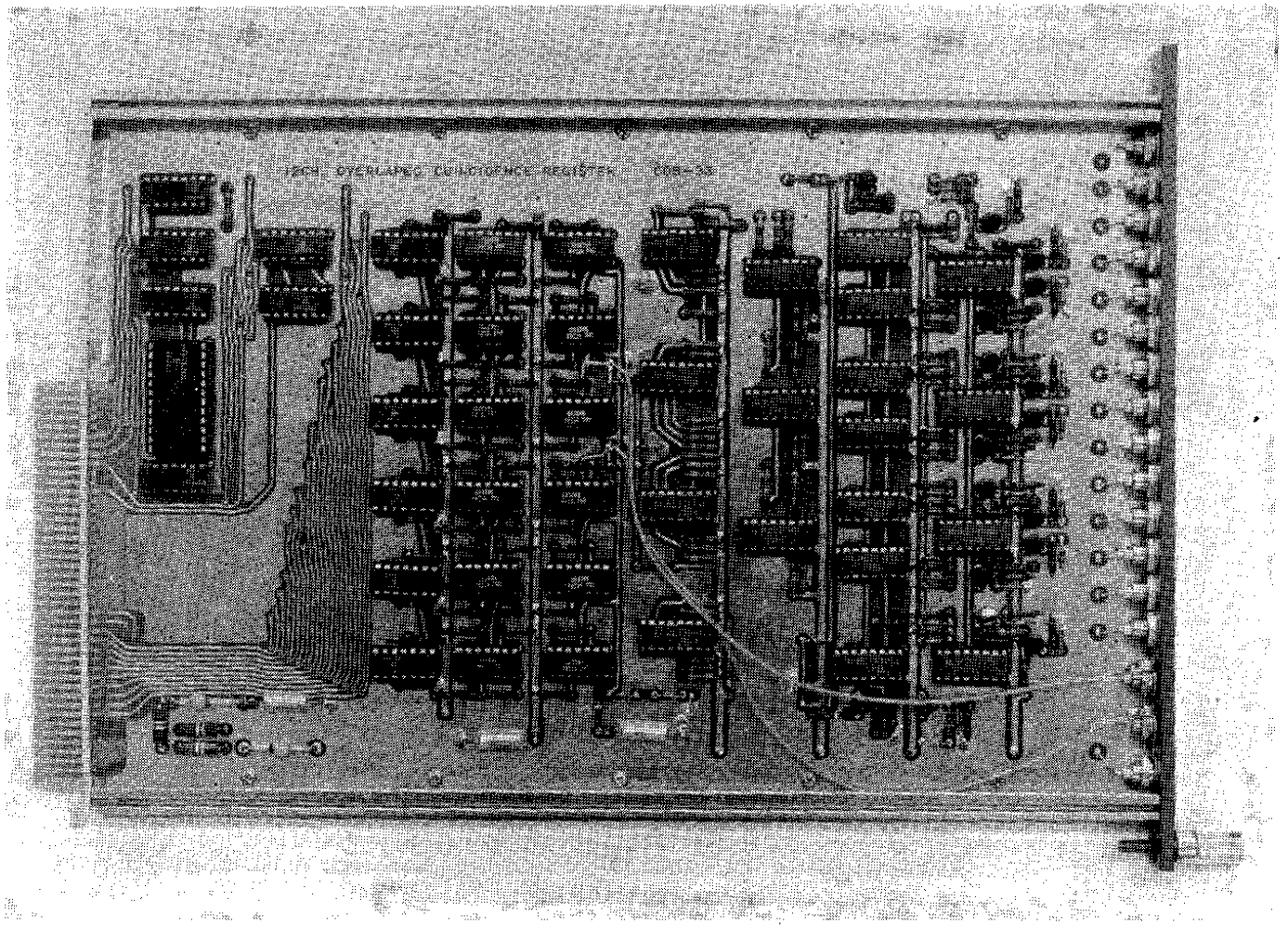


16-CH. COINCIDEGE REGISTER (2)
KEK TYPE-2 (C08-31)

C08-33 12-CH OVERLAPPED COINCIDENCE REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-33)
12-CH OVERLAPED COINCIDENCE REGISTER KEK TYPE-1



(INSIDE VIEW)
12-CH OVERLAPED COINCIDENCE REGISTER KEK TYPE-1 (C08-33)

KEK CAMAC STANDARD MODULE (C08-33) C08-33-01
12-CHANNEL OVERLAPPED COINCIDENCE REGISTER KEK TYPE-1

GENERAL

This Overlapped Coincidence Register is designed for logically treat signals from the overlapped counter hodoscope. This module accepts standard NIM fast logic signals. The logic channels, which seek a coincidence between each input and a common fast gate input, employ MECL 10K integrated circuits and provide coincidence resolving times under 2 nsec. Logical "1" data levels, representing the time coincidence between the common fast gate and the 12 inputs, are stored in a 24-bit fast buffer register for later readout under CAMAC commands.

SPECIFICATIONS

(1) Input characteristics

Inputs : 12, Lemo connectors; impedance 50 ohms ±5%; direct-coupled; protected to ±5 Volts for inputs <1 μs; reflections <10% for 2 ns risetime.

Input Threshold : Accepts standard AEC/NIM fast logic levels (-500 mV nominal).

Double Pulse Resolution : 10 ns max.; 8 ns typical.

Gate Input : One, Lemo connector; 50 ohms impedance; -600 mV or greater enables; minimum duration at full logic level (-750 mV) 2.0 ns; protected to ±5V. Should precede inputs by at least 4 ns.

Clear Input : One, Lemo connector: -600 mV or greater, 50 ohms impedance; minimum duration 10 ns; protected ±20V. 10 ns settling time after clear.

(2) Output characteristics

Data Readout : CAMAC function and address commands gate the 24 binary bits on to the 2^0 to 2^{23} CAMAC dataway bus lines; logical 1, ≤0.5 Volts (0 to 16 mA); logical 0, open circuit (≤100 μA at 5.5 Volts).

Summing Outputs : 2, Lemo connectors; high impedance bridged connectors for each set of 12 inputs; 4 mA ±3% is presented for each register latched; maximum output into 25 ohms, -1 Volt for single or cascaded units (corresponds to 10 set registers); risetime, 4 ns (increasing slightly for multiple levels); delay of leading edge of summing output from leading edge of input, 20 ns.

(3) General

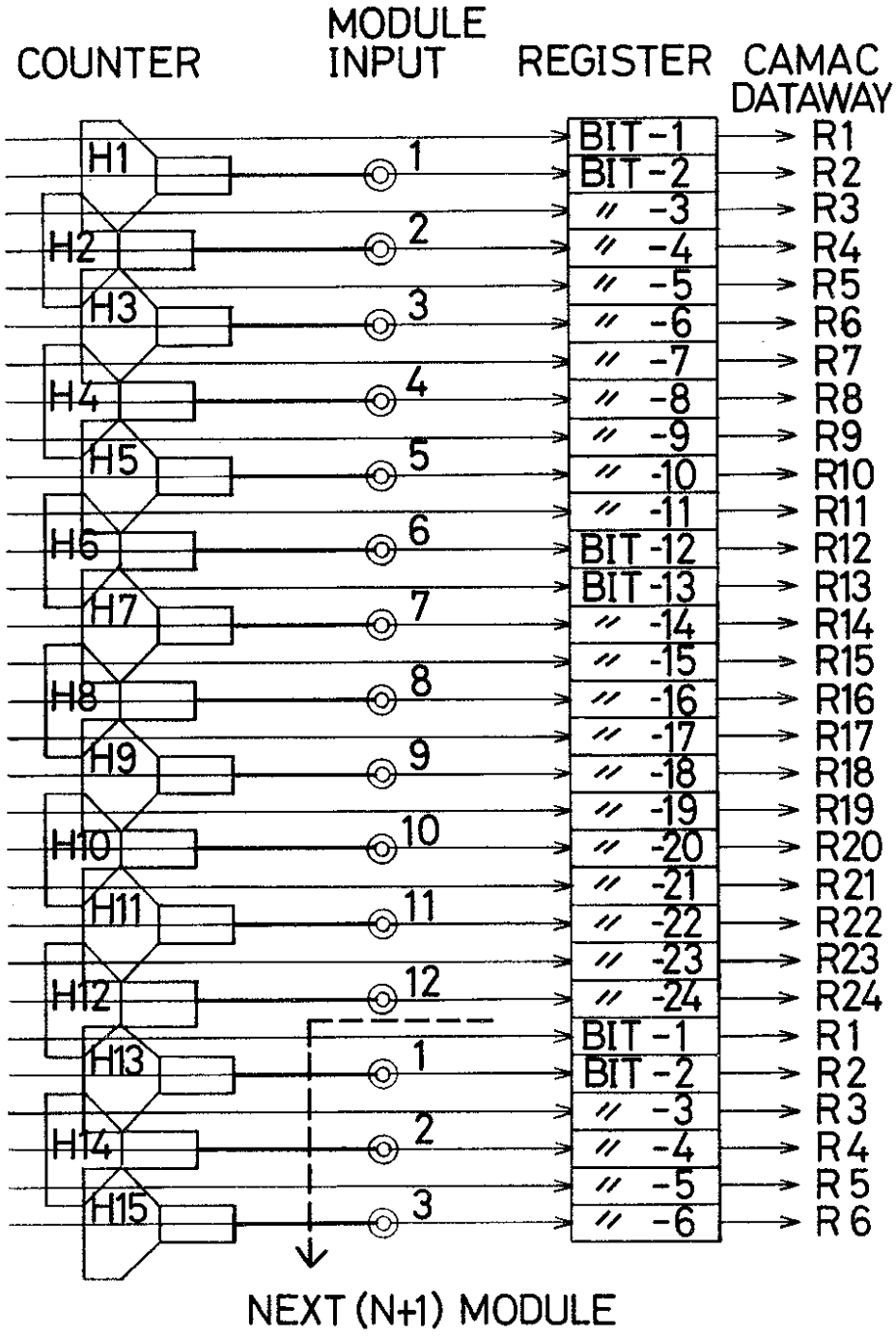
Coincidence Width : 1 ns up, determined by input and gate pulse durations.

CAMAC Commands :
- Z or C: Clears register, requires S2.
- I: Gate Input is inhibited for duration of CAMAC inhibit commands.
- Q: Q=1 response is generated in recognition of an F(0), F(2), F(9) or F(25) for a valid N and A(0), but there will be no response (Q=0) under any other condition.
- X: X=1 (Command Accepted) response is generated when a valid F, N and A command is generated.

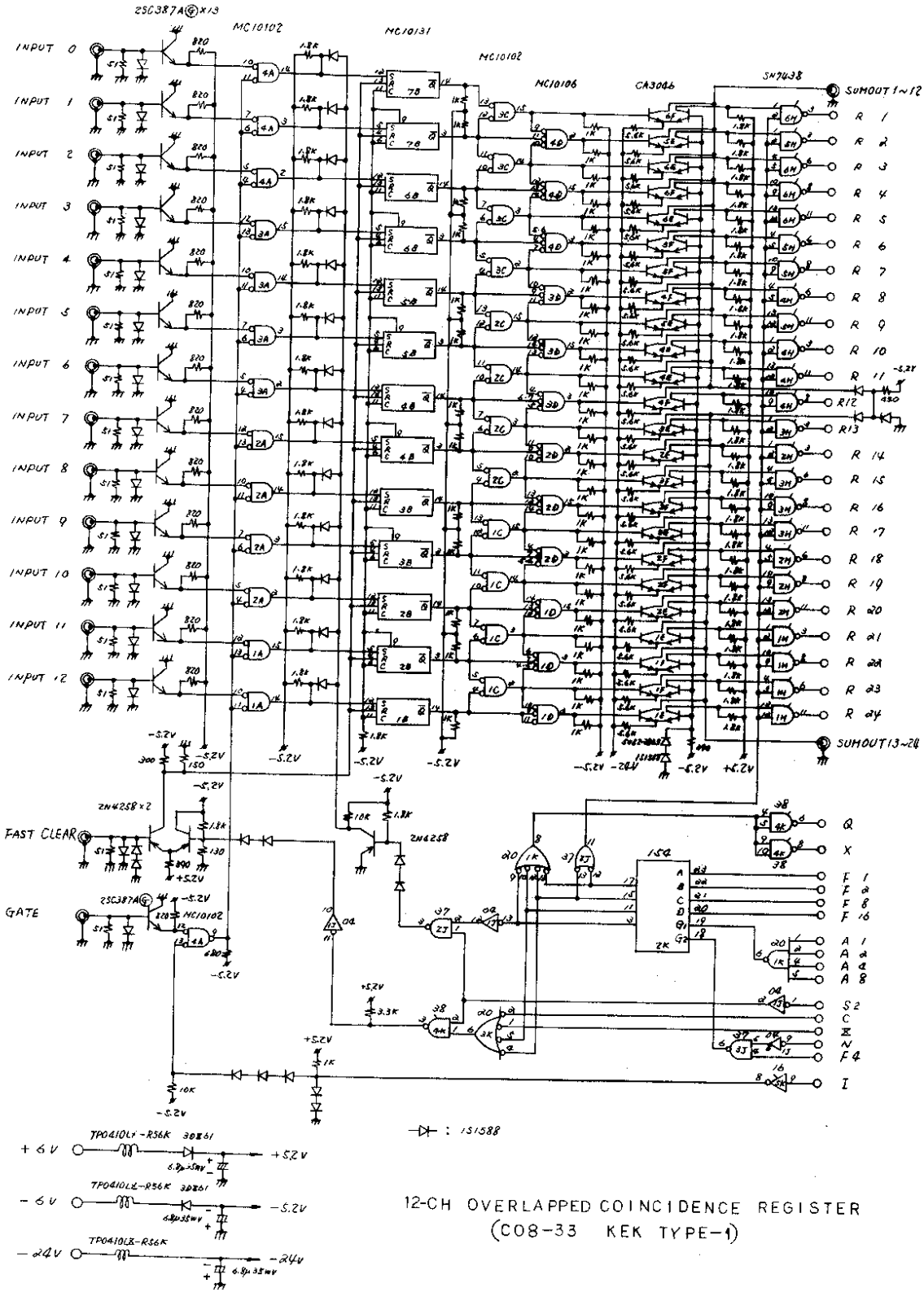
CAMAC Function Codes :
- F(0): Read group 1 register; requires N and A(0).
- F(2): Read and Clear group 1 register; requires N, A(0) and S2.
- F(9): Clear Group 1 register; requires N, A(0) and S2.
- F(25): Increment (test mode latches all channels); requires N and S2.

Packaging : CAMAC single-width module. Conforms to ESONE Report EUR 4100e standards.

Power Requirements :
+6 Volts at 610 mA;
-6 Volts at 745 mA;
-24 Volts at 280 mA.

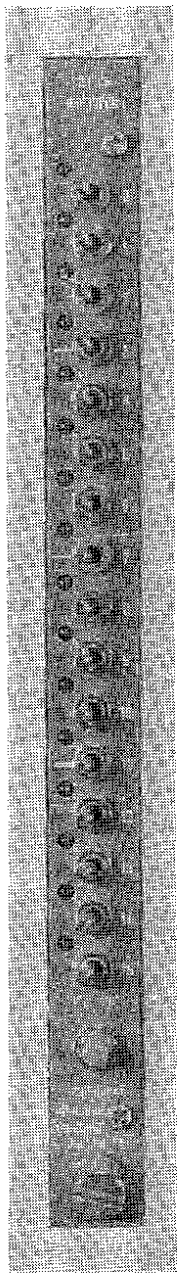


BLOCK DIAGRAM
12-CH OVERLAPPED COINCIDENCE
REGISTER KEK TYPE-1

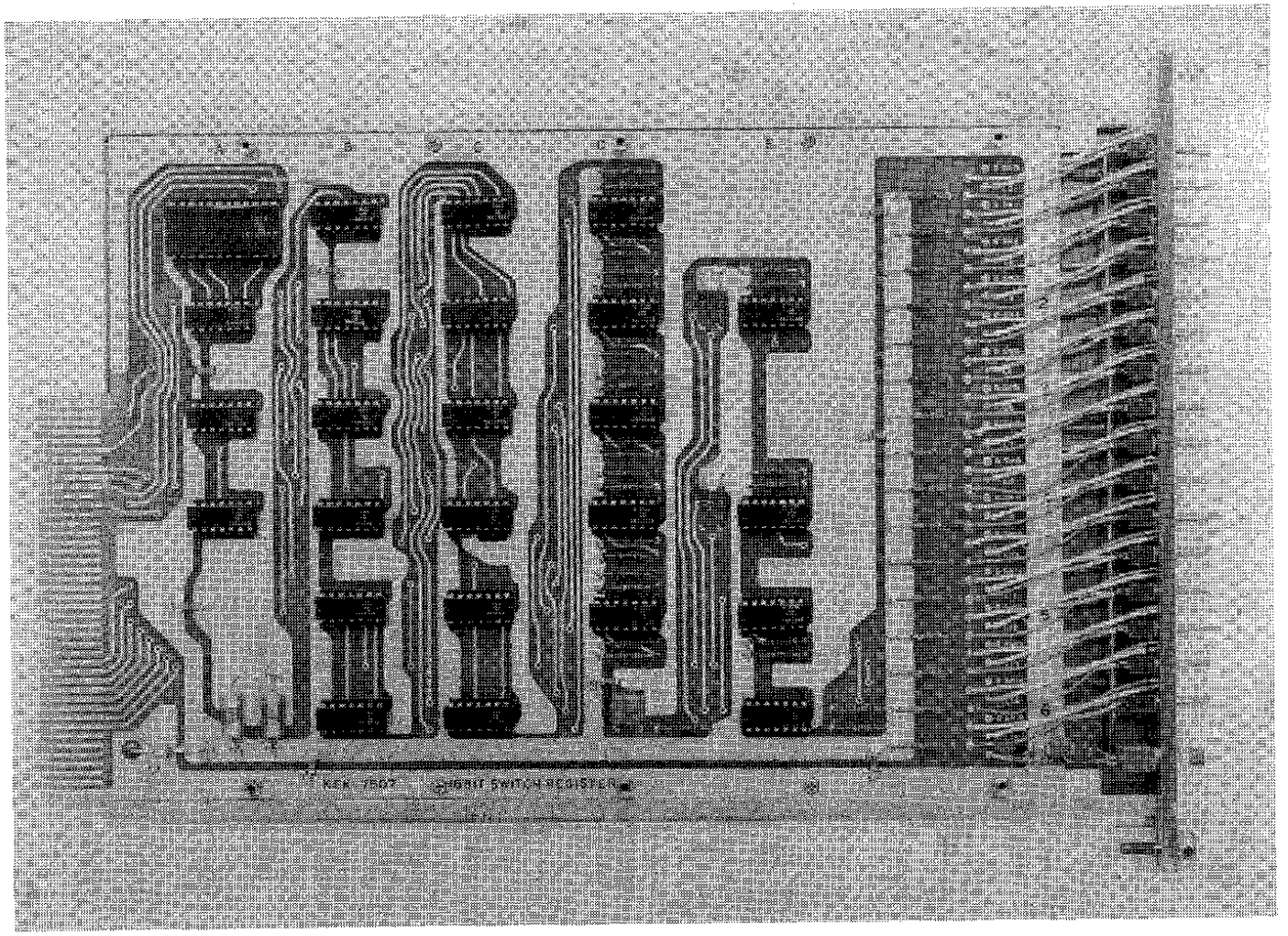


12-CH OVERLAPPED COINCIDENCE REGISTER
(CO8-33 KEK TYPE-1)

C08-41 16-BIT SWITCH REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-41)
16-BIT SWITCH REGISTER KEK TYPE-1



(INSIDE VIEW)
16-BIT SWITCH REGISTER KEK TYPE-1 (C08-41)

KEK CAMAC STANDARD MODULE (C08-41)
16-BIT SWITCH REGISTER KEK TYPE-1

GENERAL

This module provides 16 bits communication. The 16 switches can be used as

a 16-bit binary integer
a 4-digit decimal integer
16 different and independent bit informations
65536 different informations.

After setting information on each switches, the attention of the computer is called with the push-button for an interrupt request on the front panel, which generates LAM.

SPECIFICATIONS

(1) Functions

F(0)A(0) : Read 16 switches message onto R1 to R16 lines, clear the LAM at S2.
F(8)A(0) : Test LAM. Produce Q-responce, if LAM status is "on".
F(10)A(0) : Clear LAM.
F(24)A(0) : Disable LAM.
F(26)A(0) : Enable LAM.
C and Z : Disable LAM and Clear LAM.
Q responce : Q=1 for F(0)A(0) and F(8)A(0).
X responce : X=1 for all decoded functions.

(2) Front Panel

16 toggle switches

"1" is logic state "1" and LED "on".
"0" is logic state "0" and LED "off".

L-Request push-button

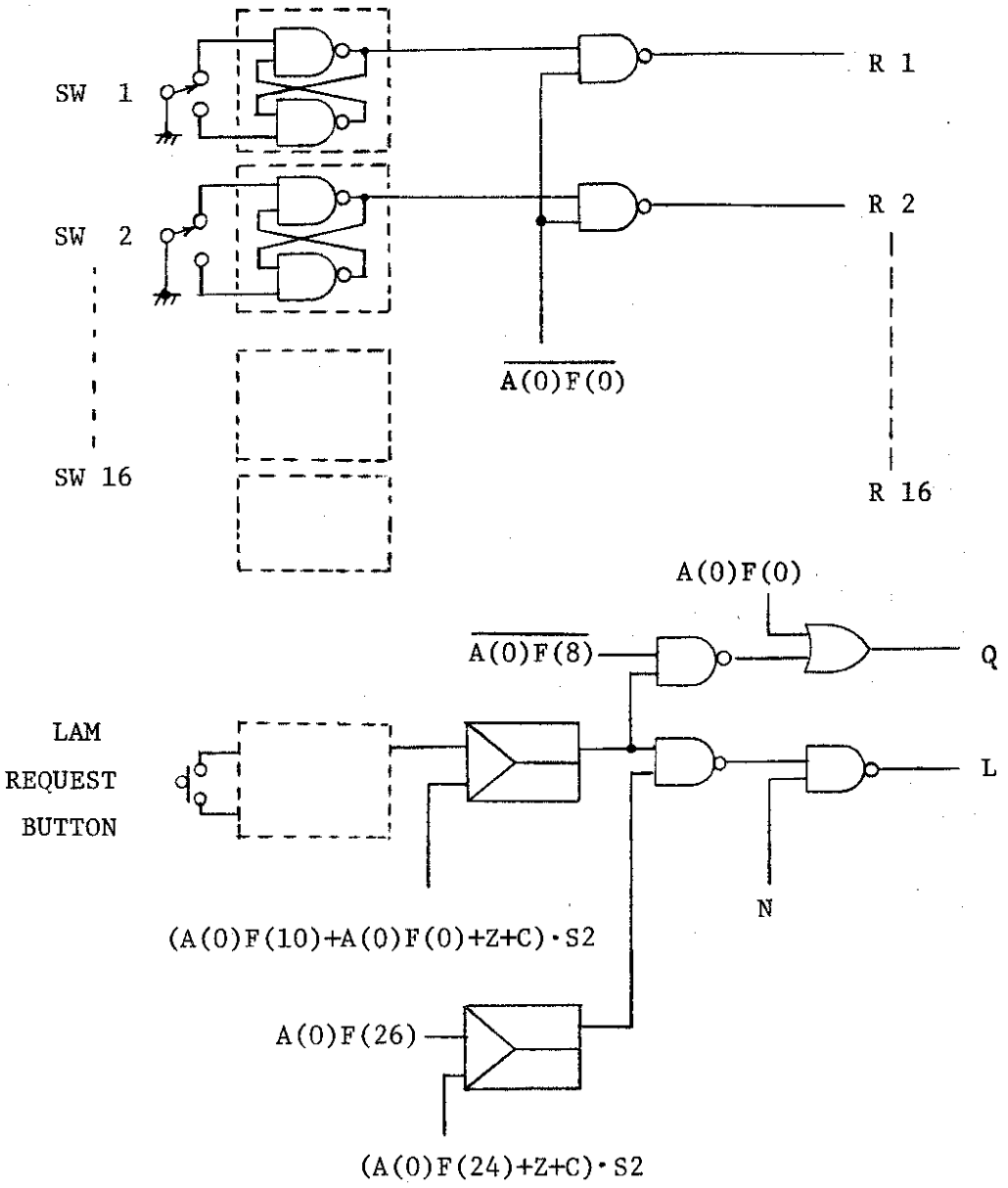
Push for requesting LAM.

(3) Power Requirement

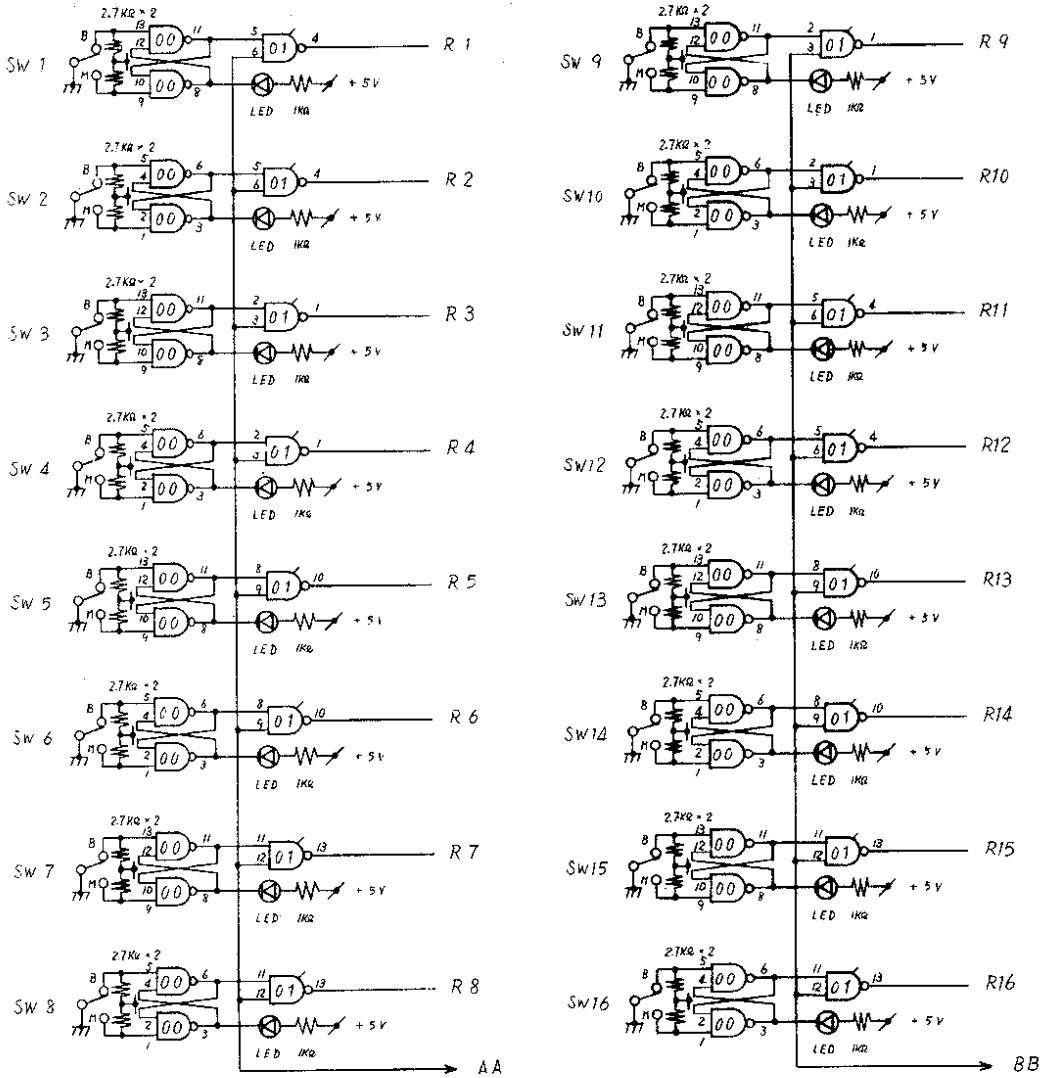
+6V : 560 mA

(4) Mechanical

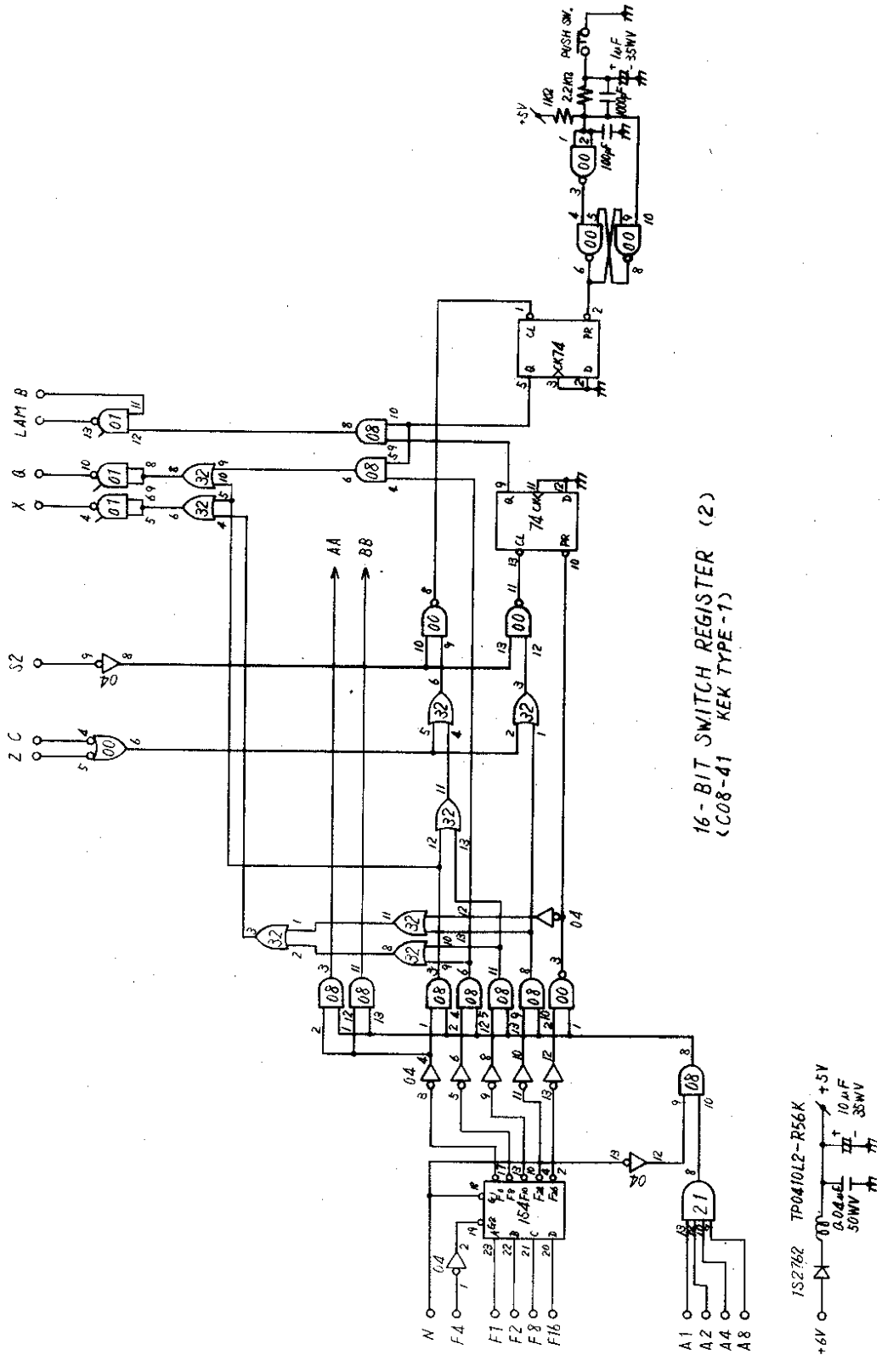
Single width CAMAC standard module.



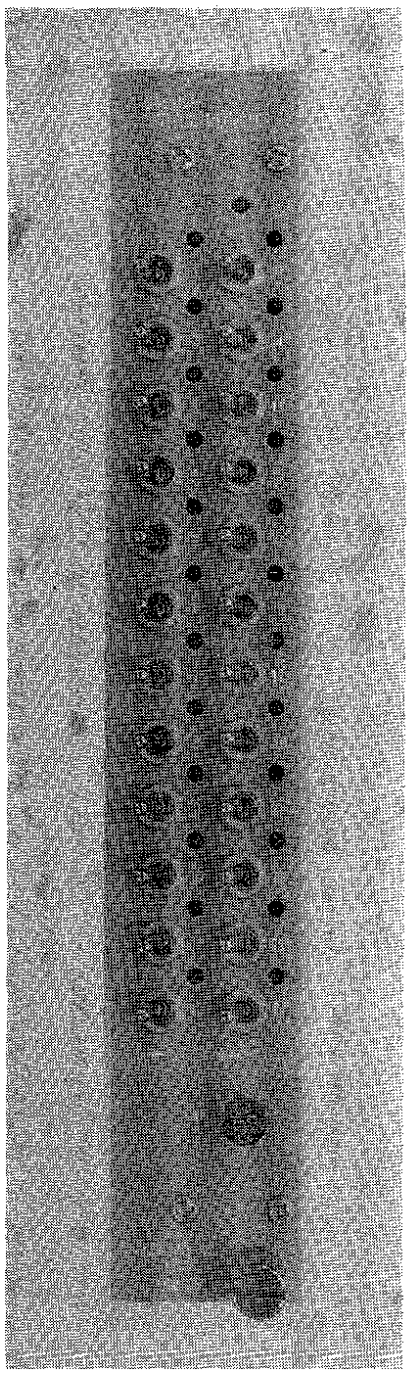
16-BIT SWITCH REGISTER BLOCK DIAGRAM
(C08-41 KEK TYPE-1)



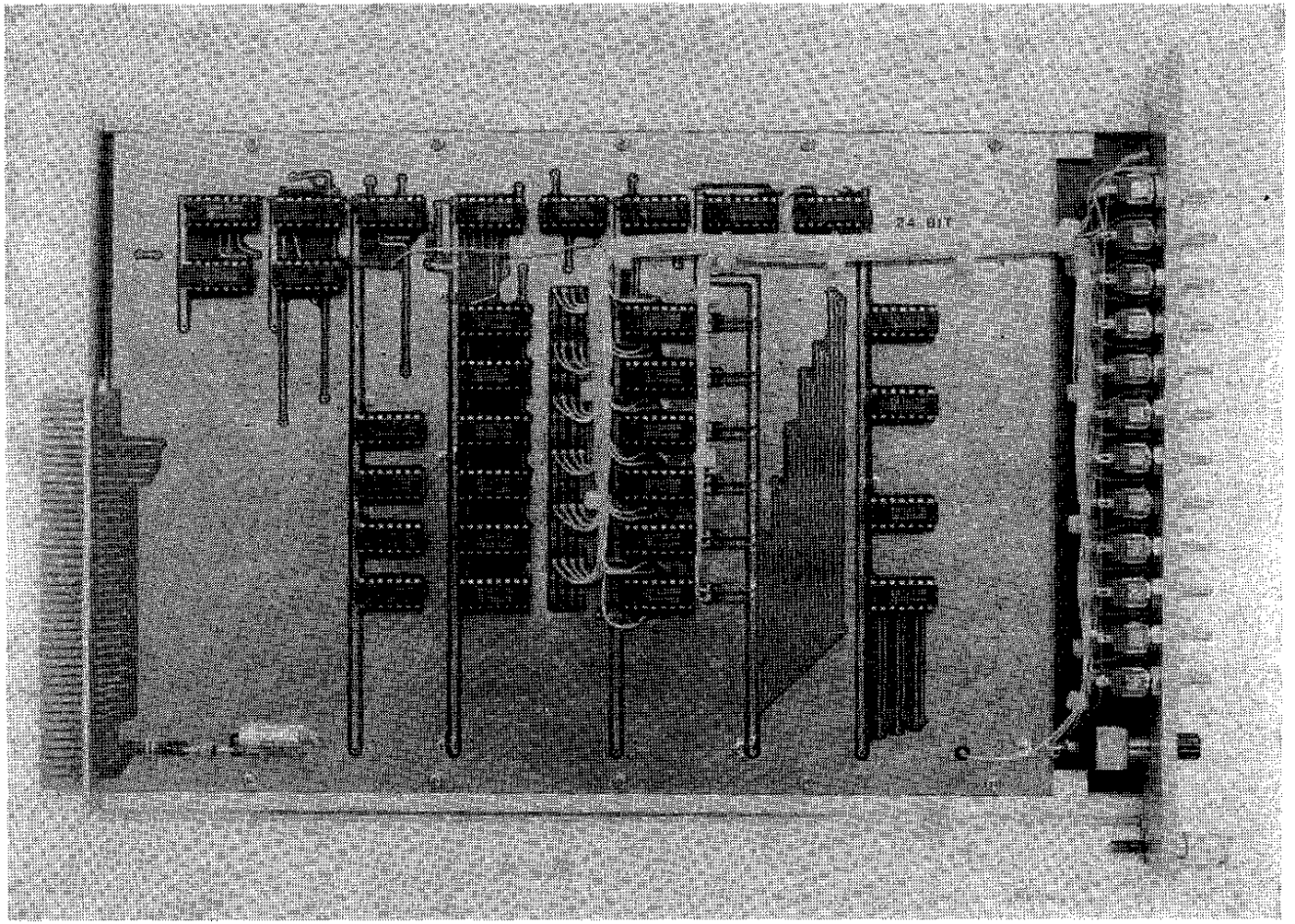
16-BIT SWITCH REGISTER (1)
(C08-41 KEK TYPE-1)


16-BIT SWITCH REGISTER (2)
(C08-41 KEK TYPE-1)
LAM B
X Q
Z C
S2
AA
BB
N
F4
F1
F2
F8
F16
A1
A2
A4
A8
PUSH SW.
1kΩ
2.2MΩ
100pF
1μF 35WV
-5V
+5V
+6V
74 CLK
CK74
TP0410L2-R56K
1S2762
0.04μF 50WV
10μF 35WV

C08-42 24-BIT SWITCH REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-42)
24-BIT SWITCH REGISTER KEK TYPE-1



(INSIDE VIEW)
24-BIT SWITCH REGISTER KEK TYPE-1 (C08-42)

KEK CAMAC STANDARD MODULE (C08-42)
24-BIT SWITCH REGISTER KEK TYPE-1

GENERAL

The 24-bit switch register has been designed to be read and written the 24-bit parallel data, which provide a simultaneous test of the CAMAC dataway lines. Specifications are almost the same as the 16-bit switch register, C08-41, except that the write mode function is available in this module.

SPECIFICATIONS

(1) Functions

F(0)A(0) : Read the 24-bit data written into the register 0 by CAMAC write mode function.
F(0)A(1) : Read the 24-bit switch status on the front panel.
F(8)A(0) : Test LAM.
F(10)A(0) : Clear LAM.
F(16)A(0) : Write into the Register 0.
F(24)A(0) : Disable LAM.
F(26)A(0) : Enable LAM.
C, Z : Clear LAM and the register 0, disable LAM.

(2) Front panel

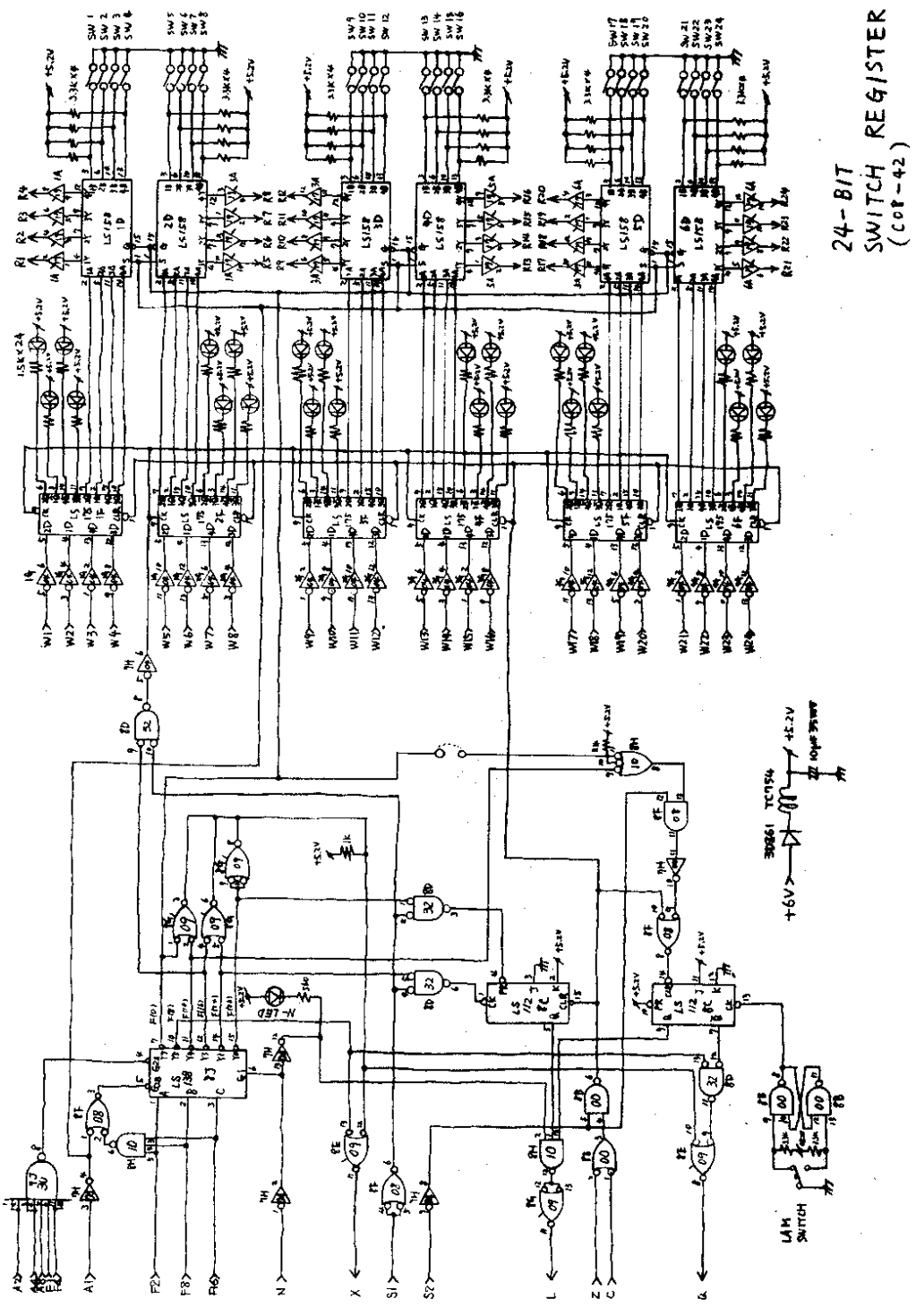
24 toggle switches can be selected either "1" or "0" corresponding to logical "1" or "0", respectively.
24 LED's indicate the status of the register 0.
"L-Request" button is used for requesting LAM.

(3) Power requirement

+6 Volts : 320mA.

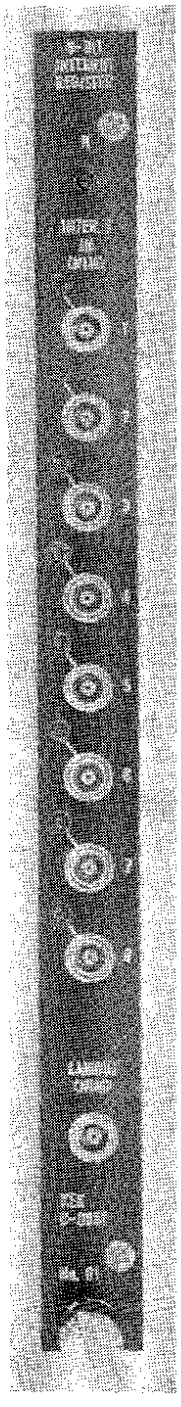
(4) Mechanical

Double width CAMAC standard module.

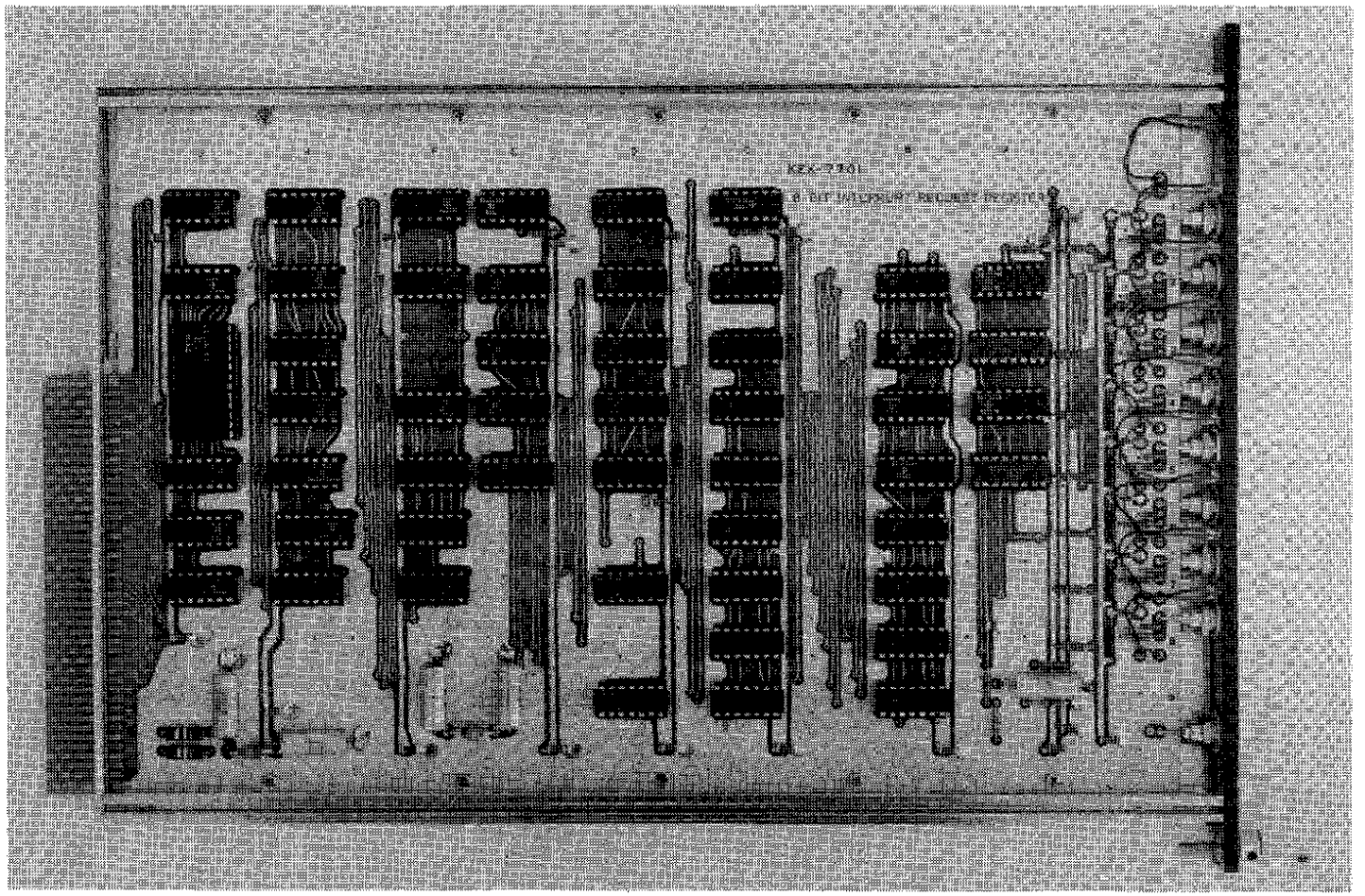


24-BIT
SWITCH REGISTER
(COR-42)

C08-51 8-BIT INTERRUPT REGISTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C08-51)
8-BIT INTERRUPT REGISTER KEK TYPE-1



(Inside View)
8-BIT INTERRUPT REGISTER KEK TYPE-1 (C08-51)

KEK CAMAC STANDARD MODULE (C08-51) C08-51-01
8-BIT INTERRUPT REGISTER KEK TYPE-1

GENERAL

This module provides a register for up to 8 externally generated interrupt reguest signals (NIM fast) to facilitate the LAM handling of the system which has various interruption sources. The LAM line is activated on receipt of any one of 8 interrupt signals. The register is read and cleared from the CAMAC dataway. Interrupts occured between CAMAC operations of read and clear are not lost. Individual bits of the register can be masked by CAMAC command.

LAM signal is also available from the LEMO connector of the front panel according to the state of the bistable which is controlled from CAMAC command.

SPECIFICATIONS

(1) Functions

F(0)A(0) : Read LAM pattern and disable LAM
F(0)A(1) : Read LAM REQUEST REGISTER
F(1)A(0) : Read LAM MASK REGISTER
F(8)A(0) : Test LAM
F(9)A(0) : Clear LAM REQUEST REGISTER
F(11)A(0) : Clear LAM MASK REGISTER
F(17)A(0) : Over write MASK REGISTER
F(21)A(0) : Selective clear LAM REQUEST REGISTER and enable LAM
F(24)A(0) : Disable LAM
F(24)A(1) : Disable LAM output from front panel
F(26)A(0) : Enable LAM
F(26)A(1) : Enable LAM output from front panel
C : Clear LAM REQUEST REGISTER
Z : Clear LAM REQUEST REGISTER, LAM MASK REGISTER, and disable LAM
Q response : F(0)A(0) + F(0)A(1) + F(1)A(0) + F(17)A(0) + F(21)A(0) or LAM·F(8)A(0)
X response : All accepted CAMAC functions

(2) Front panel

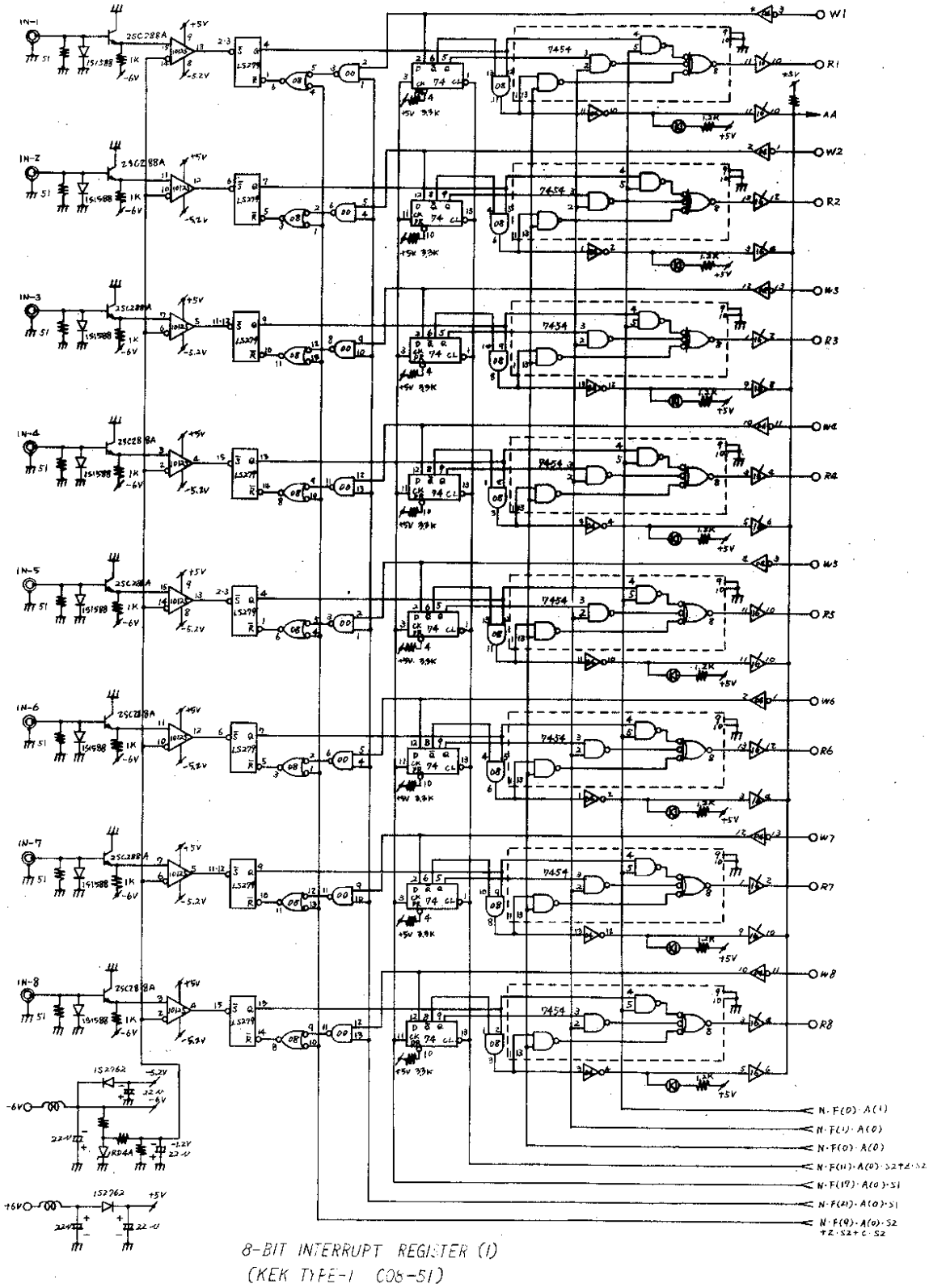
INTER'T IN : "INTER'T IN" from 1 to 8 accept interrupt signal from external source with NIM logic level. The associated LED is on if the interrupt is accepted (i.e. not masked).
LAM OUT : The "LAM" output is available if enabled by F(26)A(1).

(3) Power requirement

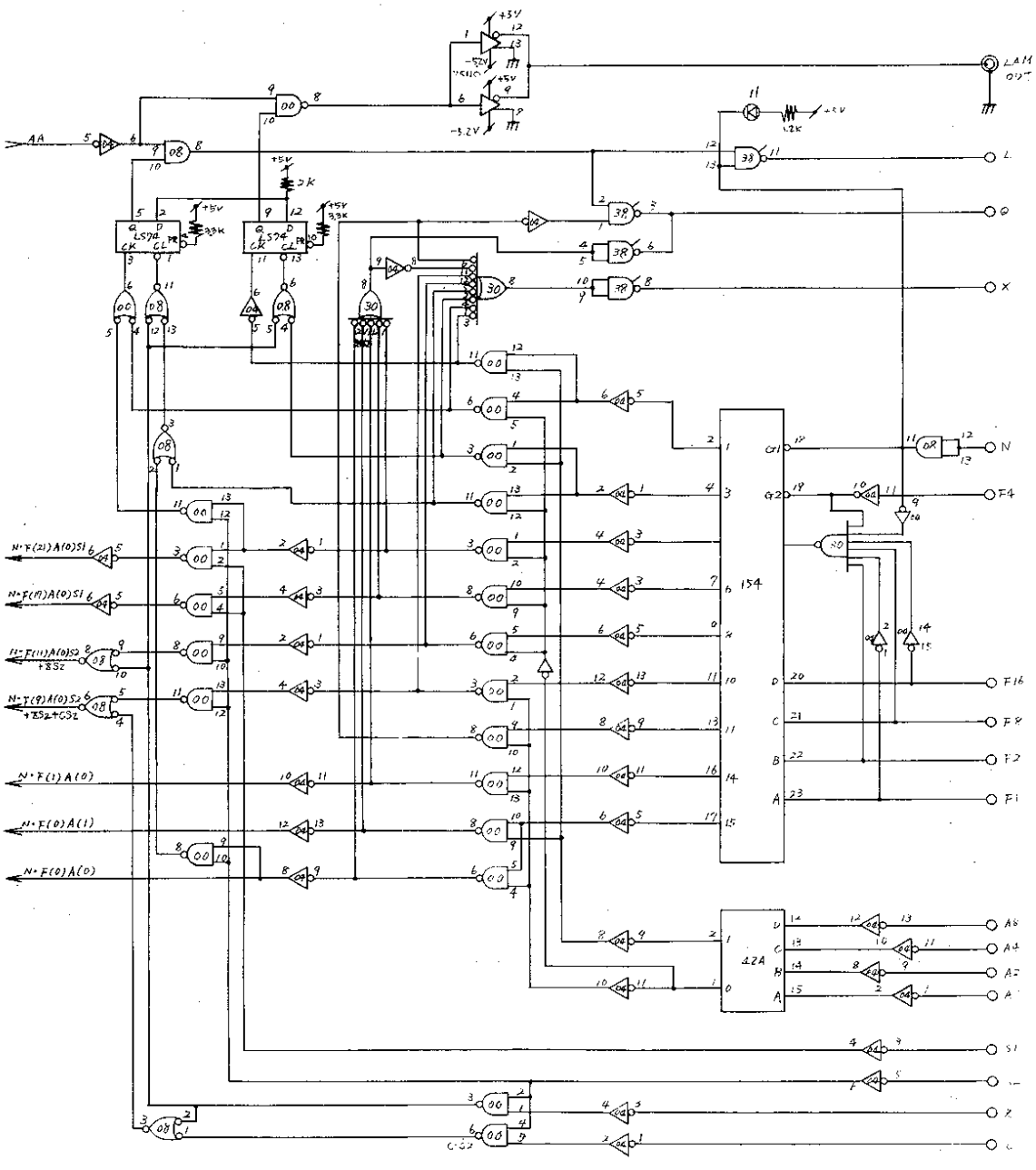
+6V : 720mA
-6V : 170mA

(4) Mechanical

single width CAMAC standard module.

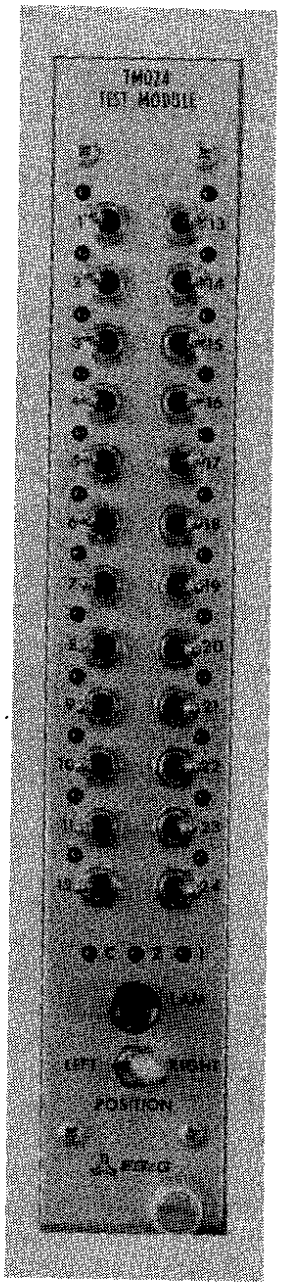


8-BIT INTERRUPT REGISTER (1)
(KEK TYPE-1 C08-51)



8-BIT INTERRUPT REGISTER (2)
(PEK TYPE-1 CCC-51)

C08-60 TEST MODULE (EGG TM 024)



KEK CAMAC MODULE (C08-60)
TEST MODULE

KEK CAMAC STANDARD MODULE (C08-60) C08-60-01
TEST MODULE (EGG TM024)

DESCRIPTION

The TM024 BD-Test Module is a system analysis tool packaged as a CAMAC-standard double-width module for use in testing a CAMAC crate Dataway and its module interfaces at any two adjacent module stations in the crate except those occupied by the crate controller. With the TM024, malfunctions in the system can be isolated down to modular level. All system interconnections are made by the two CAMAC Dataway connectors on the rear of the module, and there are no front panel connectors. The TM024 conforms fully to the requirements of Specification EUR 4100e.

The module consists of two identical printed-circuit boards, each of which is connected to the CAMAC Dataway through a CAMAC-standard Dataway connector. The two boards are interconnected by 53 jumpers, each of which interconnects a point in the circuit on one board with the corresponding point in the circuit on the other board. The front panel indicator lights and switches are common to the two boards. A two-position (Left-Right) locking toggle switch on the front panel selects either board.

Each of the two boards is connected to the 24 Dataway W lines, the 24 Dataway R lines, the 4 Dataway A lines, the 5 Dataway F lines, and the Dataway B, L, N, Q, I, C, Z, S1, S2, +6V dc, and ground lines at the crate module station at which it is installed. On each board a 24-binary-bit storage register is provided for the data word fed to that board on the 24 Dataway W lines. The outputs of each of the two storage registers are gated into the 24 Dataway R lines and to the 24 front panel bit monitoring lights.

There are 24 front panel two-position toggle switches for feeding a 24-binary-bit data word to the 24 Dataway R lines at the proper command. Front panel indicator lights are provided for visual monitoring of the Dataway I, C, and Z lines. A front panel momentary-contact push-botton switch provides the capability of manually generating a Dataway L-line Look-at-Me (LAM) signal when the Dataway B-line Busy signal is absent. Each board has the circuitry for decoding the Dataway N-, F-, and A-line signals and for utilizing the Dataway S1- and S2-line Strobe signals for timing purposes and for generating the Dataway Q-line Response signal.

SPECIFICATIONS

(1) CONTROLS AND INDICATORS

(a) Controls

Left-Right Position (S26) : Front panel 2-position toggle switch determines which of the two printed-circuit boards is enabled and which

is disabled; in the Right position, enables right board and disables left board; in the Left position, enables left board and disables right board.

LAM (S25) : Front panel momentary-contact push-button switch generates Dataway L-line Look-at-Me signal through either board, as determined by the position of the front panel Position switch, whenever the Dataway B-line Busy signal is absent.

Bit Switches (S1-S24) : 24 front panel two-position toggle switches allow any manually selected 24-binary-bit data word to be fed from the module to the crate controller via the Dataway R lines; collectively, these switches are known as the "switch register".

(b) Indicators

I, C, Z : Front panel monitoring lights respectively monitor the Dataway I, C, and Z lines; whenever a signal is present on any of these three lines, the corresponding monitoring light will be lit.

Bit Monitoring Lights : 24 front panel monitoring lights permit continuous visual monitoring of the data word contained in the storage register of either board, as determined by the position of the front panel Position switch; although these lights are located adjacent to the front panel bit switches, there is no relationship between the indication of each light and the position of the adjacent bit switch; when lit, each light indicates that its corresponding bit in the storage register has a value of binary 1.

(2) DATA INPUTS

Twenty-four Dataway W lines through rear panel CAMAC-standard-Dataway connector. W1 carries least significant bit (LSB); W24 carries most significant bit (MSB).

(3) CONTROL INPUTS

(a) Dataway Lines

C and Z : Signal on either will light its corresponding front panel monitoring light and will reset the storage registers of both boards to zero; neither of these signals is dependent on the position of the front panel Position switch or on the Dataway S2-line Strobe signal.

I : Signal on this line will light the front panel I monitoring light.

B : Signal on this line will disable the generation of a Dataway L-line Look-at-Me signal.

(b) CAMAC Codes

A(0) : Storage register subaddress.
A(1) : Switch register subaddress.
F(0) : Read register selected by subaddress.
A <2 : Q=1, A> 1 : Q=0.
F(2) : Read register selected by subaddress and clear storage register; uses S2.
A <2 : Q=1, A> 1 ; Q=0.
F(6) : Read module characteristic; does not use A; Q = 1.
F(9) : Clear storage register; uses S2.
A=0 : Q=1, A> 0 : Q=0.
F(16) : Write into storage register; uses S1.
A=0 : Q=1, A> 0 : Q=0.

(4) OUTPUTS

Data Outputs : 24 Dataway R lines through rear panel CAMAC-standard-Dataway connector. R1 carries LSB; R24 carries MSB.

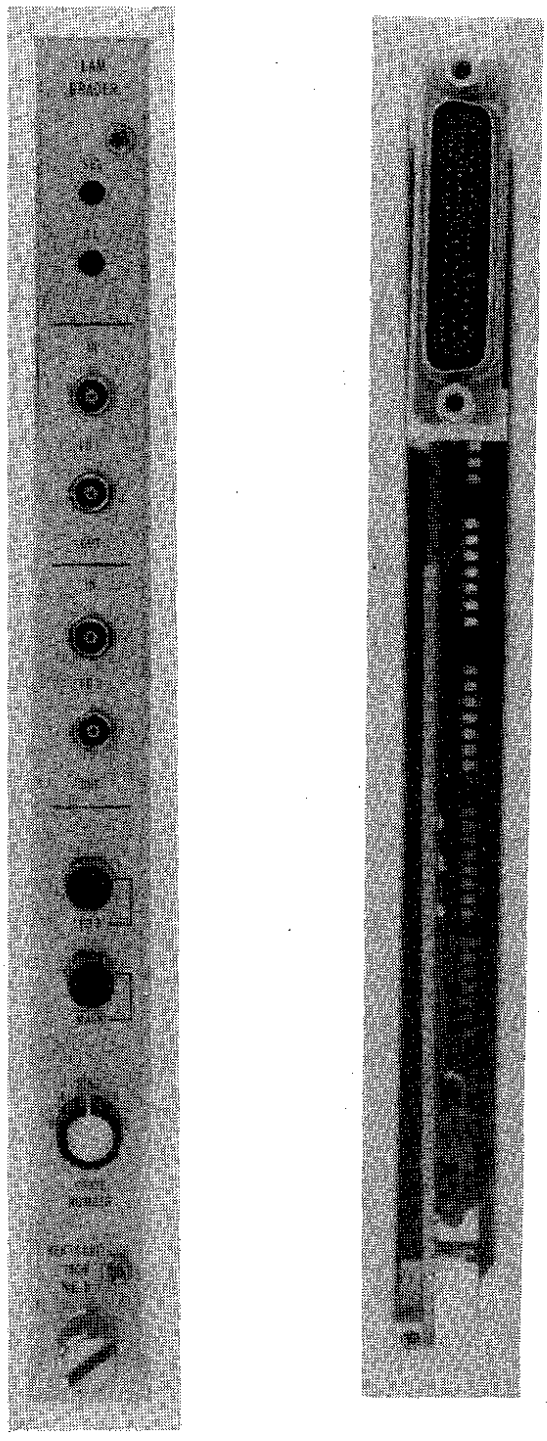
Q : Signal generated by TM024 and carried out through rear panel CAMAC-standard-Dataway connector on Q line in response to valid function code, subaddress, and N-line signal.

L : Look-at-Me signal generated by manually depressing the front panel LAM switch in the absence of the Dataway B-line Busy signal and carried out through rear panel CAMAC-standard-Dataway connector on L line.

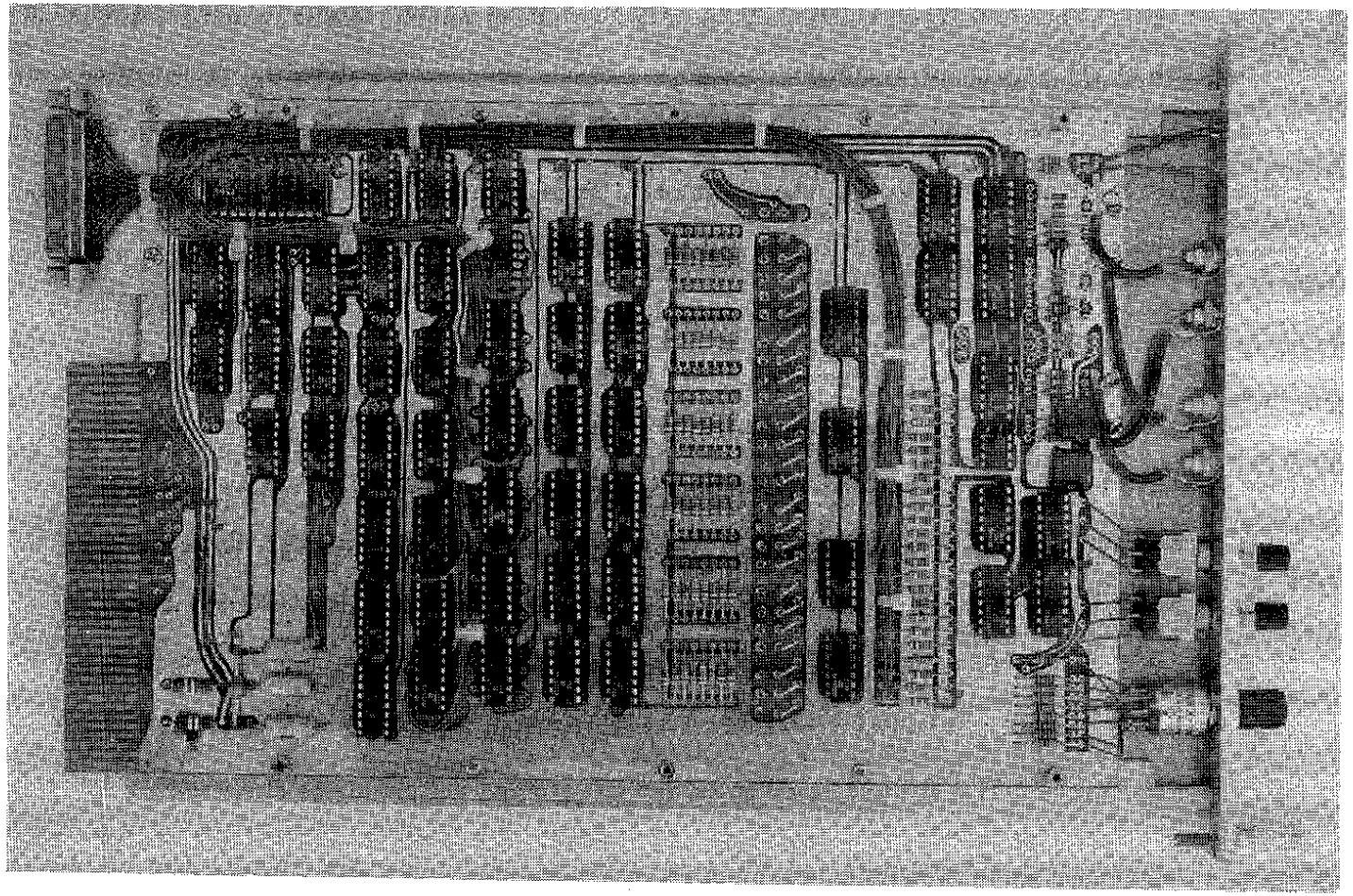
(5) POWER REQUIREMENTS

+6V at 1000mA.

C09-11 LAM GRADER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C09-11)
LAM GRADER KEK TYPE-1



(Inside View)
LAM GRADER KEK TYPE-1 (C09-11)

KEK CAMAC STANDARD MODULE (C09-11) C09-11-01
LAM GRADER KEK TYPE-1

GENERAL

The Lam Grader is designed for treat the LAM request signals within a crate through the standard crate controller type-A1 (CCA1) according to EUR 4600e. The Lam Grader must be connected to CCA1 through the rear panel connector by a 26-pair-twisted cable. This Lam Grader has specific functions as follows.

(A) The individual LAM signals from normal stations and the front panel of this module can be arranged to form a 24-bit Graded LAM word (GL-word) using a jumper wiring on the printed circuit board. The bits of GL word are OR'ed in the crate controller in order to generate Branch Demand (BD) for the Branch Driver.

(B) The module has a 24-bit MASK register to facilitate masking LAM request from undesired GL bits. The MASK register is written by CAMAC function, or un-masked by the front panel push button MASK.

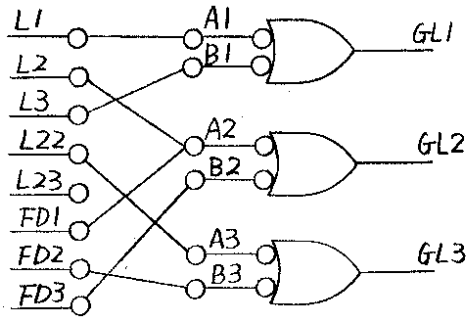
(C) The GL word is read by two types of CAMAC functions, (a) GL operation (BG): the GL words of all on-line crates are OR'ed to form a single GL pattern which is read into the computer, and (b) CAMAC read function (F(0)): the each GL word in a crate is read out by CAMAC function: CN(30)A(1-7)F(0).

(D) This Lam Grader is designed based on the KEK specification to be used in a multi-crate system. In a multi-crate system, the number of the crate which generated Branch Demand is directly transfered in a GL word by the GL operation if the crate number switch on the front panel has been set. The GL within a crate is read by the CAMAC function CN(30)A(1-7)F(0).

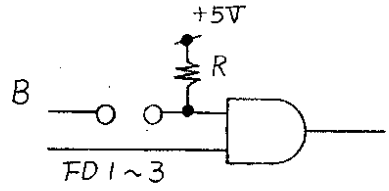
SPECIFICATIONS

(1) Patch Connection

The individual LAM request signal must be connected with a jumper wire in order to form a GL word in a crate. Any type of connection shown below is available.



As an option the Demand from the front panel can be gated with B signal of CAMAC dataway by wiring the patch points on the printed circuit boad.



(2) CAMAC Functions

GL operation

(1) Single crate mode

The Crate Number Switch is on SING. The LAM words of all on-line crates are OR'ed and read into the computer.

(2) Multi-crate mode

The crate number switch on the front panel is set on the number equal to that of the associate crate. The number of the crate which generated BD is set on a lower seven bits (1-7) of the GL word and read by GL operation.

CN(30)F(0)A(0) : (1) Single Crate Mode.

Read the GL word of the crate.

(2) Multi Crate Mode.

Read the GL word which contains crate number bit corresponding to crates which have generated BD.

CN(30)F(0)A(1-7) : Read GL word of the crate.
CN(28)F(10)A(0) : Clear FPD1 LAM.
CN(28)F(10)A(1) : Clear FPD2 LAM.
CN(28)F(10)A(2) : Clear FPD3 LAM.
CN(28)F(16)A(0) : Over write MASK register.
Logical "1" corresponds to un-mask,
logical "0" corresponds to mask.
Z : Clear Mask Register (mask) and FPD1, FPD2, FPD3 LAM.
Q-response : Generated (Q=1) for N(28)F(16)A(0).

X-response : Generated (X=1) for N(28)F(10)A(0-2) and N(28)F(16)A(0).

(3) Front Panel

FD1 and FD2 : Input, Lemo connector, impedance 50 ohms. This Front Panel Demand input accepts a NIM fast logic signal to generate LAM from the external LAM request. Output, Lemo connector. This Output provides a NIM fast logic signal. Quiescently 0 mA, -16 mA (-800 mV into 50 ohms load) during output.

FD3 (push-button switch) : The manual demand FD3 (interrupt) can be generated by pushing the button.

$\overline{\text{MASK}}$ (push-button switch) : Actuation sets Demand Mask register to "un-masking" condition.

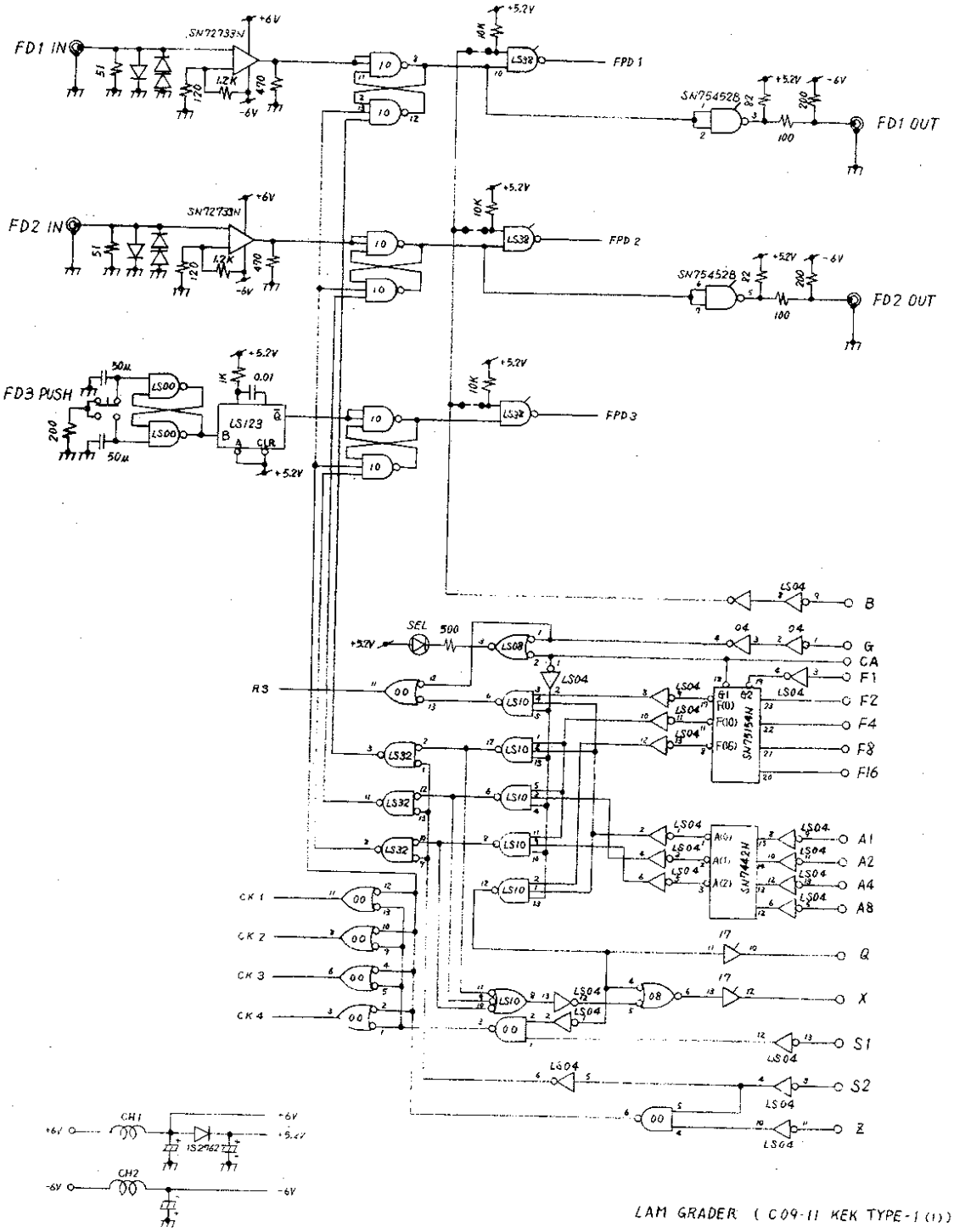
CRATE NUMBER (rotary switch) : SING: Single Crate Mode.
1-7: Crate Number for Multi-crate Mode.

(4) Rear Panel

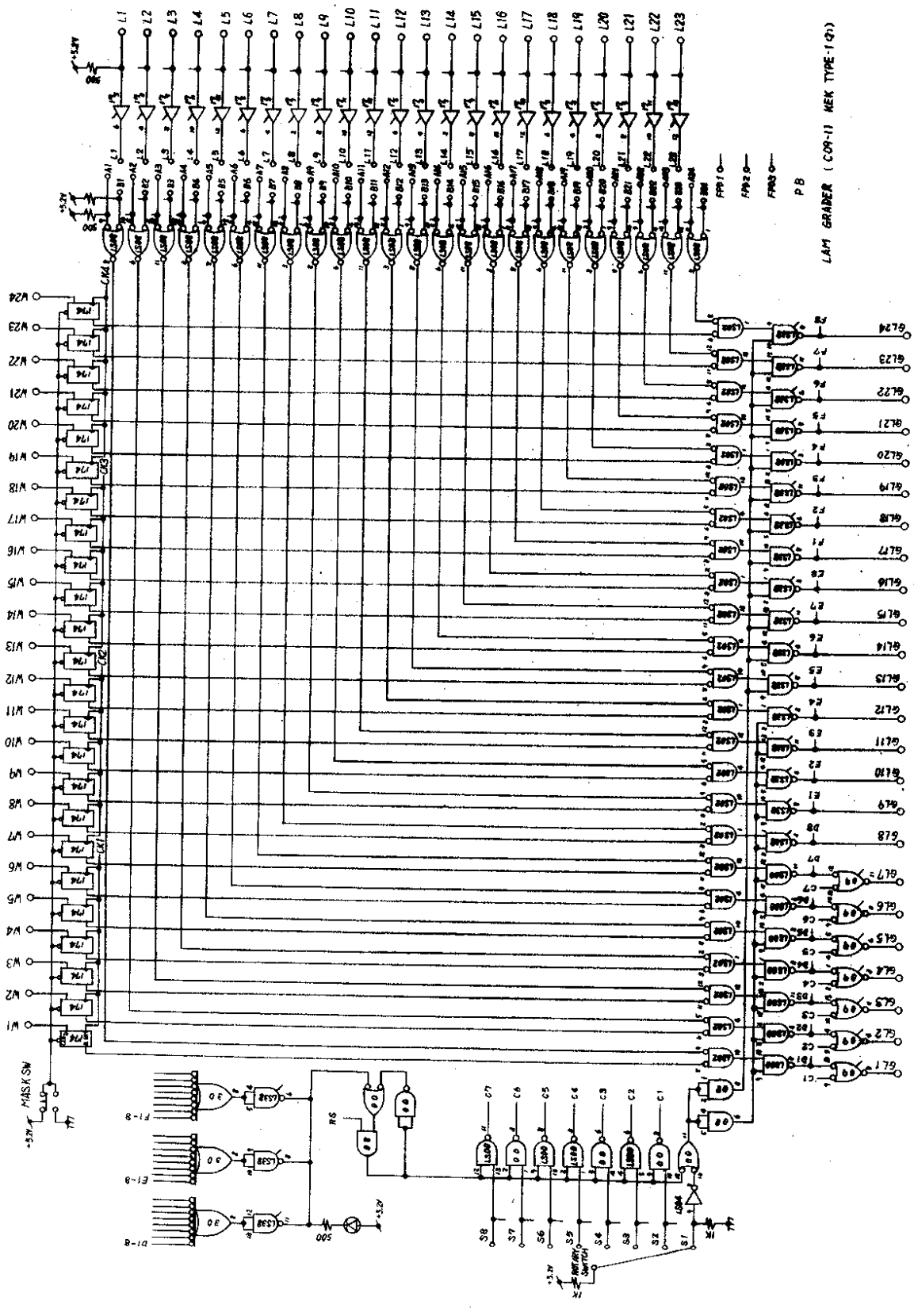
CCA Connector : A 52-way Cannon Double Density connector (type 2DB52S) mounted within the free-access area of the crate provides link to the CCA. For pin allocation see Table below.

(5) Packaging : CAMAC single width module. Conforms to ESONE Report EUR 4100e standards.

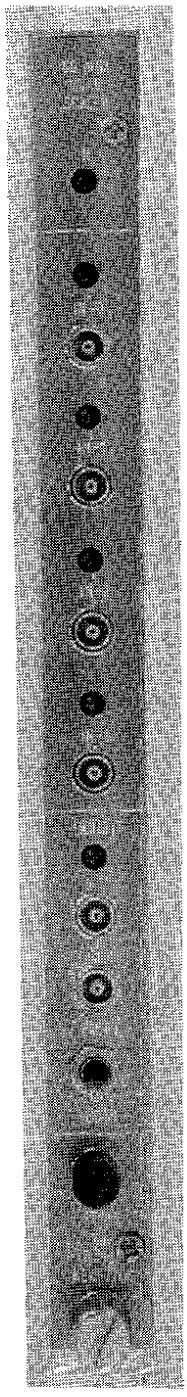
(6) Power Requirements : +6 Volts : 640 mA.
-6 Volts : 75 mA.



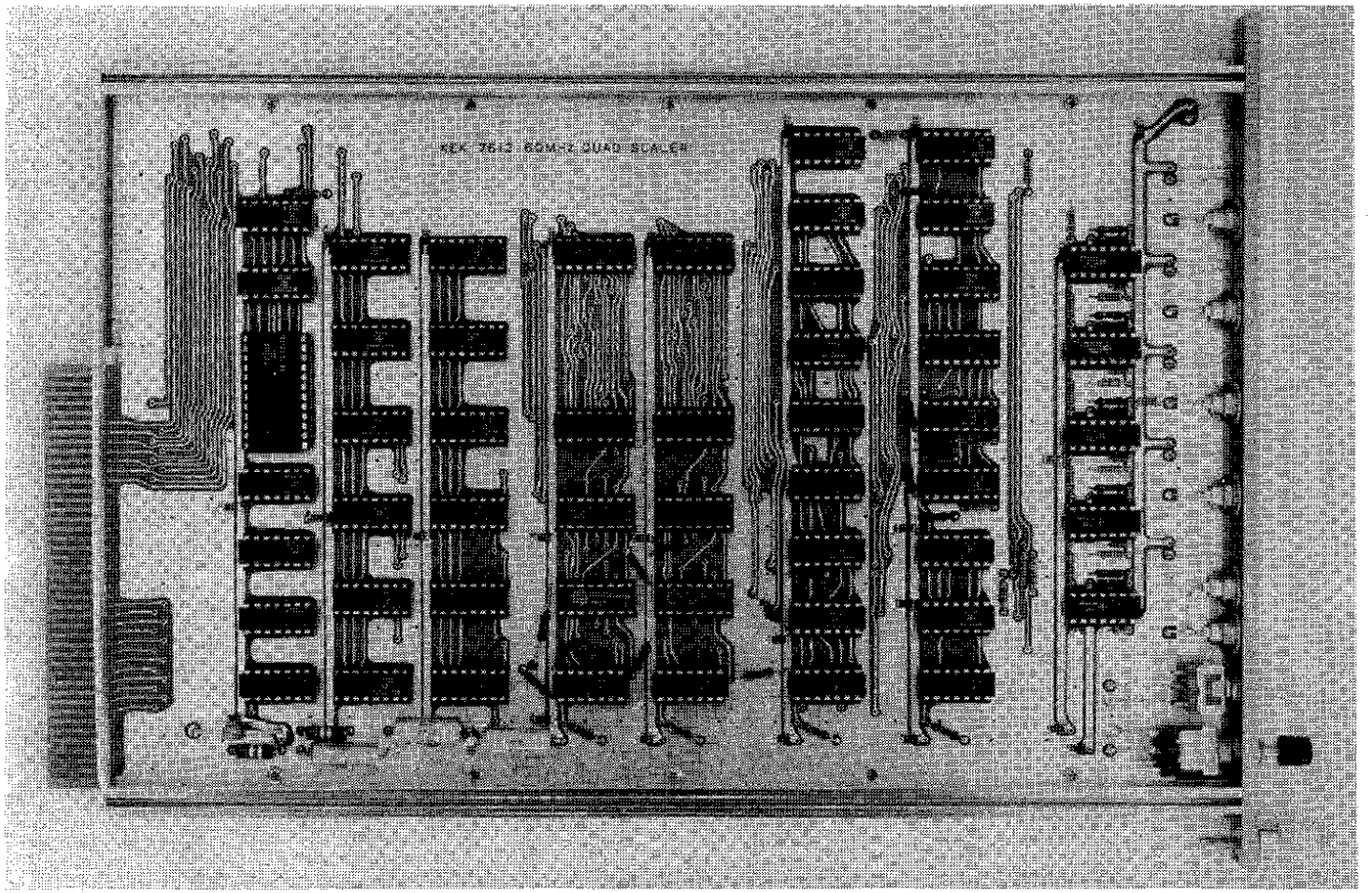
LAM GRADER (C09-11 KEK TYPE-1 (1))


LAM GRADER (COG-11 KEK TYPE-1 Ch)
P B
MASK SW
ROTARY SWITCH

C10-12 QUAD BINARY 80 MHz SCALER (KEK TYPE-2)



KEK CAMAC STANDARD MODULE (C10-12)
QUAD BINARY 80MHz SCALER KEK TYPE-2



(INSIDE VIEW)
QUAD BINARY 80MHz SCALER KEK TYPE-2 (C10-12)

KEK CAMAC STANDARD MODULE (C10-12) C10-12-01
QUAD BINARY 80MHz SCALER KEK TYPE-2

GENERAL

This module contains four identical 24-bit binary scalers. Each scaler is equipped with an extremely wideband input circuit which responds to NIM fast logic signals of any duration down to 6 nsec. The ability to recognize narrow input signals at an equivalent rate of 80MHz is an important feature.

This module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 80MHz. The CAMAC Inhibit (I) provides inhibit control via the rear dataway connector.

SPECIFICATIONS

(1) Signal input

Number of Channels : Four.
Threshold Level : -400mV (NIM fast logic levels).
Impedance : 50 ohms, direct-coupled.
Minimum Pulse Width : 6 nsec FWHM at -800mV input amplitude.
Multiple Pulse Resolution : 12.5 nsec.
Counting Rate : DC to 80MHz.

(2) Signal inhibit

Common input, -400mV threshold level, 6 nsec minimum input width, impedance 50 ohms.

(3) Overflow flag

Any scaler generates LAM signal when 24th bit produces the overflow signal.

(4) Count capacity

24 binary bits (16, 777, 216).

(5) Function codes

F(0)A(0-3) : Read registers, A(0) through A(3) are used for channel addresses.
F(2)A(0-3) : Read registers and clear module.
F(8)A(0-3) : Test Look-at-Me, Q response is generated if LAM is set.
F(9)A(0-3)S2 : Clear registers, requires only one from A(0) to A(3).
F(10)A(0-3)S1 : Clear Look-at-Me, requires only one from A(0) to A(3).

F(25)A(0-3) : Increment all scalers, requires any A from A(0) to A(3).

(6) Commands

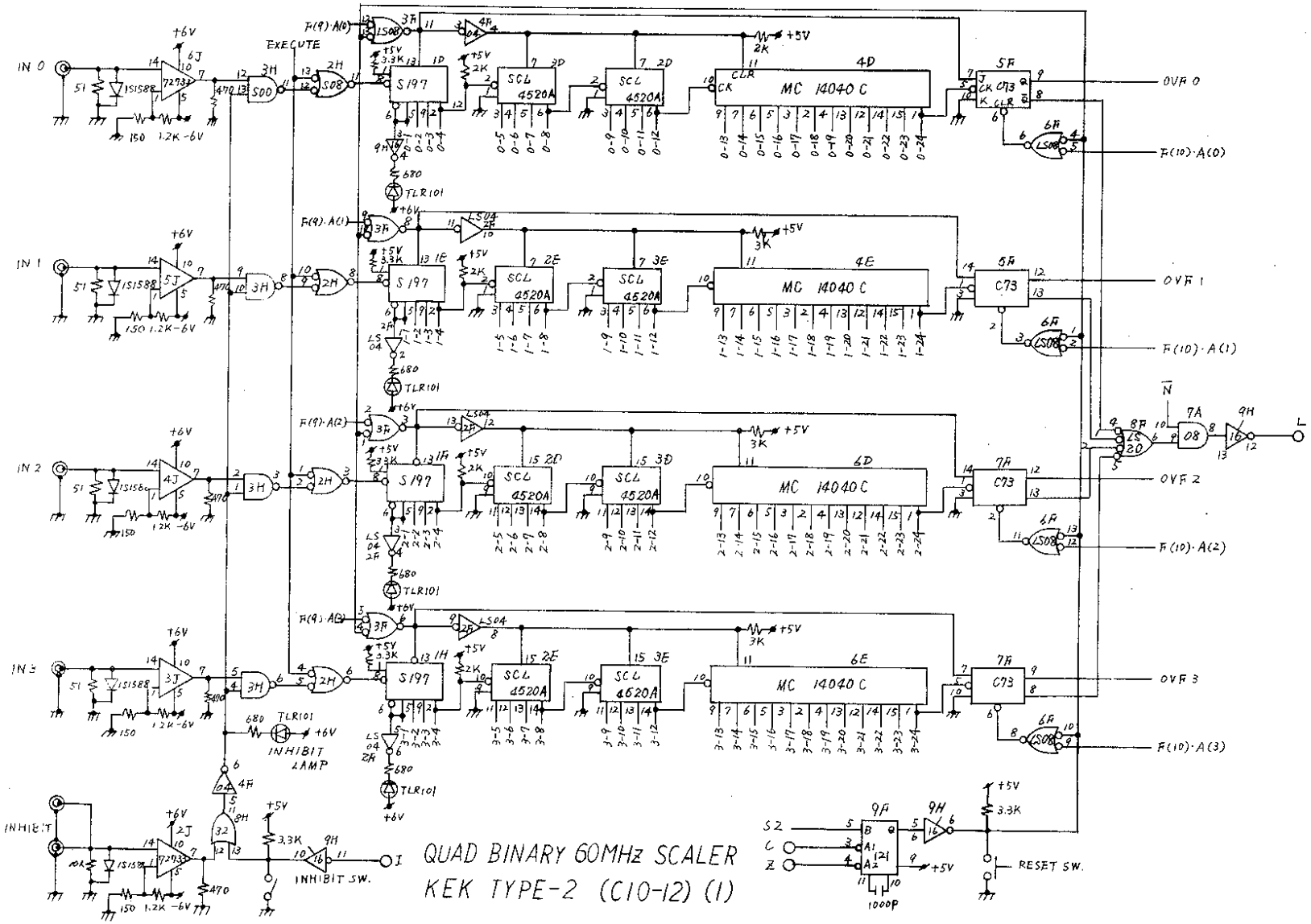
C : All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command.
Z : Same as C command.
I : All scaler inputs are inhibited during CAMAC "Inhibit" command.
L : A Look-at-Me signal is generated from time when first 24th bit produces the overflow signal until C, Z or F(10) command. LAM is disabled for the duration of N, and can be tested by F(8) Test LAM.

(7) Packaging

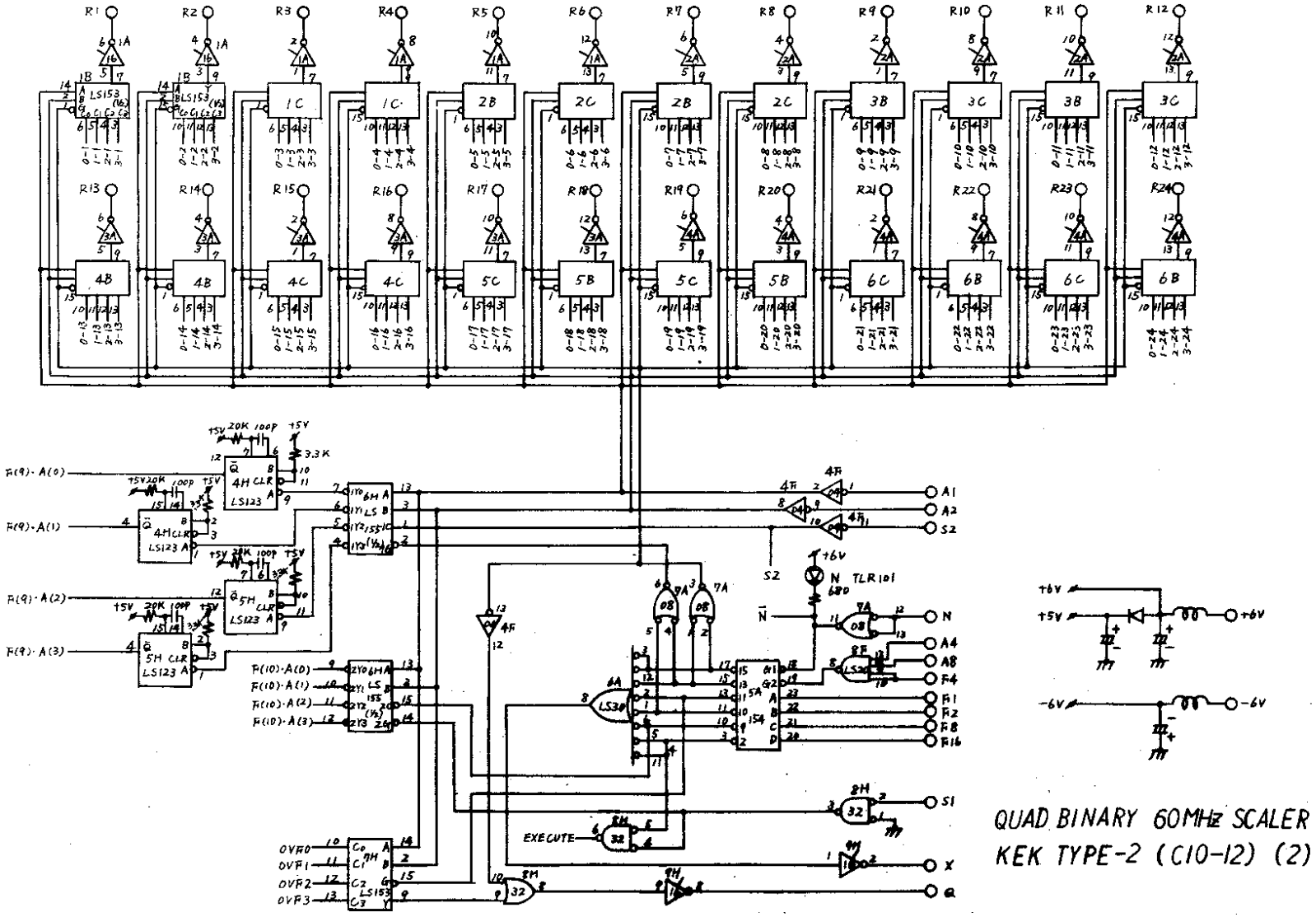
In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC single width module.

(8) Current requirements

+6 Volts : 730mA.
-6 Volts : 100mA.

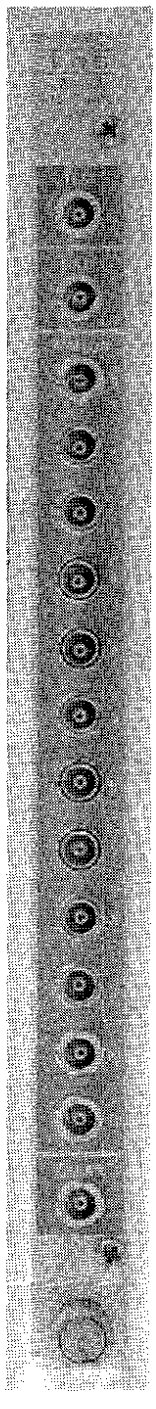


QUAD BINARY 60MHz SCALER
KEK TYPE-2 (C10-12) (1)



QUAD BINARY 60MHz SCALER
KEK TYPE-2 (C10-12) (2)

C11-10 12-CH ANALOG TO DIGITAL CONVERTER (LECROY 2249A)



KEK CAMAC STANDARD MODULE (C11-10)
12-CH ANALOG TO DIGITAL CONVERTER (LeCROY 2249A)

KEK CAMAC STANDARD MODULE (C11-10) C11-10-01
12-CH ANALOG TO DIGITAL CONVERTER (LECROY 2249A)

SPECIFICATIONS

(1) ANALOG INPUTS:

Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4mV; 50Ω impedance; linear range normally -2mV to -1V; protected to ±50 volts against 1 μsec transients.

(2) FULL-SCALE RANGE:

256 pC.

(3) FULL-SCALE UNIFORMITY:

±5%

(4) INTEGRAL NON-LINEARITY:

±.25% of reading ±0.5pC. Set of linearity curves for all channels supplied with each unit.

(5) ADC RESOLUTION:

10 bits actual, (0.1%).

(6) LONG-TERM STABILITY:

Better than 0.25% of reading ±0.5 pC/week (at constant temperature).

(7) TEMPERATURE COEFFICIENT:

Typical, 0; max., ±[.03% of reading (in pC) +.002t] pC/C (where t = gate duration in nanoseconds, with 50Ω reverse termination).

(8) ADC ISOLATION:

A 5-volt, 20ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25pC.

(9) GATE INPUT:

One gate common to all ADCs; LEMO-type connectors; 50Ω impedance; -600mV or greater enables; minimum duration, 10ns; maximum recommended duration, 200ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy), effective opening and closing times: 2ns; internal delay, 2ns.

(10) FAST CLEAR: C11-10-02

One front-panel input common to all ADC's; LEMO-type connector; 50Ω impedance; -600mV or greater clears, minimum duration, 50ns. (Caution: narrower pulses cause partial clearing) Requires additional 2.0μs settling time after clear.

(11) RESIDUAL PEDESTAL:

Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50Ω reverse termination.

(12) TEST FUNCTION:

With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of -12.5pC/volt into all inputs at F(25)·S2 time. (With CAMAC I not present, F(25)·S2 will generate the 80ns gate only, providing a measure of residual pedestal only.)

(13) DIGITIZING TIME:

60μs. By factory option, 8-bit operation at 12.5μs digitizing time may be provided.

(14) READOUT TIME:

Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.

(15) READOUT CONTROL:

Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.

(16) DATA:

The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.

(17) CAMAC COMMANDS:

Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.)

Q:AQ=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.)
X:An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
L:A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.

(18) CAMAC FUNCTION CODES:

F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses.
F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.)
F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set.
F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11).
F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(25): Test module; requires N, S2, and any A from A(0) to A(11).
F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.

(19) Q AND LAM SUPPRESSION:

Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channles contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

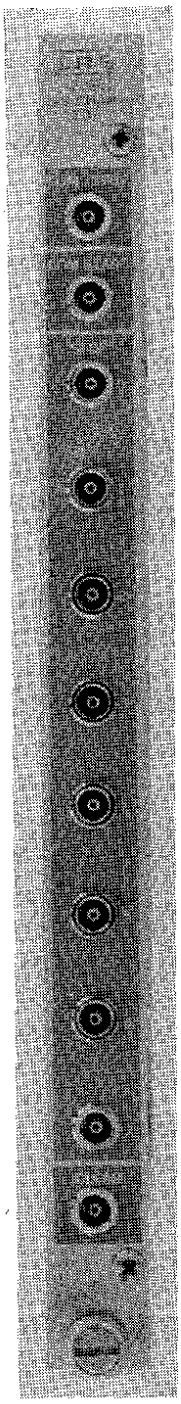
(20) PACKAGING :

In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e).
RF shielded CAMAC #1 module.

(21) CURRENT REQUIREMENTS :

+24 Volts at 35mA ;
-24 Volts at 15mA ;
+6 Volts at 850mA ;
-6 Volts at 200mA .

C11-20 OCTAL TIME TO DIGITAL CONVERTER
(LeCroy 2228A)



KEK CAMAC STANDARD MODULE (C11-20)
OCTAL TIME TO DIGITAL CONVERTER (LeCROY 2228)

KEK CAMAC STANDARD MODULE (C11-20)
OCTAL TIME TO DIGITAL CONVERTER (LeCROY MODEL 2228)

SPECIFICATIONS

(1) STOP INPUTS:

8, one per channel; 50Ω impedance; Lemo-type connectors; direct-coupled; input amplitude>-600mV; ineffective unless preceded by a "Start" input.

(2) COMMON START INPUT:

One, common to all channels; 50Ω impedance; Lemo-type connector; input amplitude> -600mV.

(3) COMMON STOP INPUT:

One, common to all channels; 50Ω impedance; Lemo-type connector; > -600mV; functions identical to individual "Stop Inputs" above; used for precision on-line testing.

(4) FAST CLEAR:

One input common to all channels; Lemo-type connector; 50Ω impedance; -600mV or greater clears, minimum duration, 50 ns (requires additional 2.0 μs settling time after clear).

(5) FULL-SCALE TIME RANGE:

10-bit binary output corresponds to 102 ns, 204 ns, and 510 ns, switch selectable (with longest range field adjustable up to 1 μsec). Larger full-scales possible by factory option at slight expense of accuracy and stability, giving 1 μsec, 2 μsec, and 5 μsec as the 3 switch-selectable time ranges.

(6) INTEGRAL NON-LINEARITY:

±2counts (10 ns to full scale). Set of linearity curves for all channels supplied with each unit.

(7) TIME RESOLUTION:

100 ps on 102 ns range; 200 ps on 204 ns range; 500 ps on 510 ns range.

(8) TEMPERATURE COEFFICIENT:

Typically (+0.02% of full scale ±0.01% of reading) per degree C.

(9) DIGITIZING TIME:

50 μsec; conversion is initiated by receipt of "Start" input.

(10) READOUT TIME:

Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.

(11) TEST FUNCTIONS:

An internal start/stop is generated by F(25) with ≈75 ns spacing. Precision on-line testing and calibrating can be done with common start and common stop above.

(12) DATA:

The proper CAMAC function and address command gates the 10 binary bits plus overflow bit of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines.

(13) CAMAC COMMANDS:

Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2".
I: "Start" input is inhibited during CAMAC "Inhibit" command.
Q: AQ=1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition.
The Q response for empty modules is suppressed (see Q and LAM suppression).
X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
L: A Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed by empty modules.

(14) CAMAC FUNCTION CODES:

F(0): Read registers, requires N and A. A(0) through A(7) are used for channel address.
F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only.
F(8): Test Look-At-Me; requires LAM, N, and any A from A(0) to A(7) independent of Disable Look-At-Me. Q is generated if LAM is present.

F(9): Clear module (and LAM); requires N and A, and S2.
F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(7).
F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7).
F(25): Test module; requires N, S2, and any A from A(0) to A(7).
F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(7). Remains enabled until Z or F(24) applied.
Caution: The state of the LAM mask will be arbitrary after power turn-on.

(15) Q AND LAM SUPPRESSION:

A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

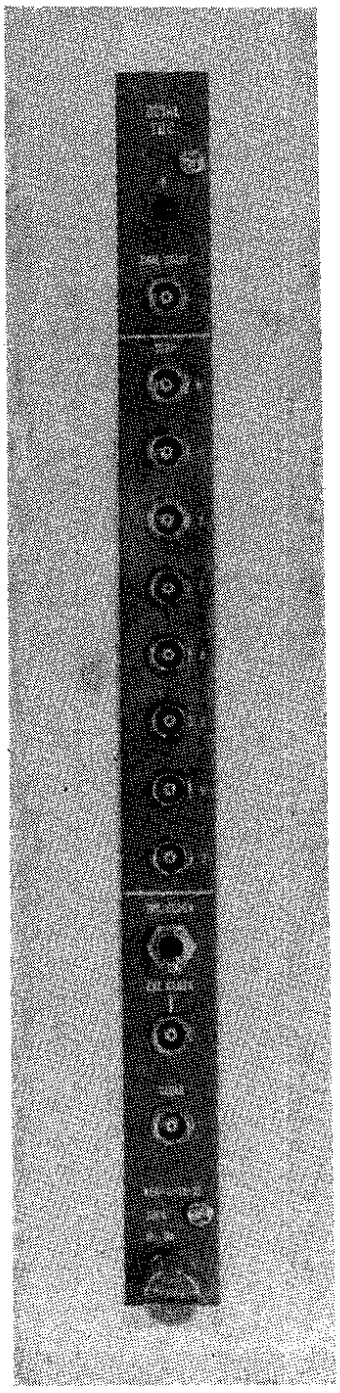
(16) PACKAGING:

In conformance with CAMAC standard for nuclear modules. RF-shielded CAMAC#1 module.

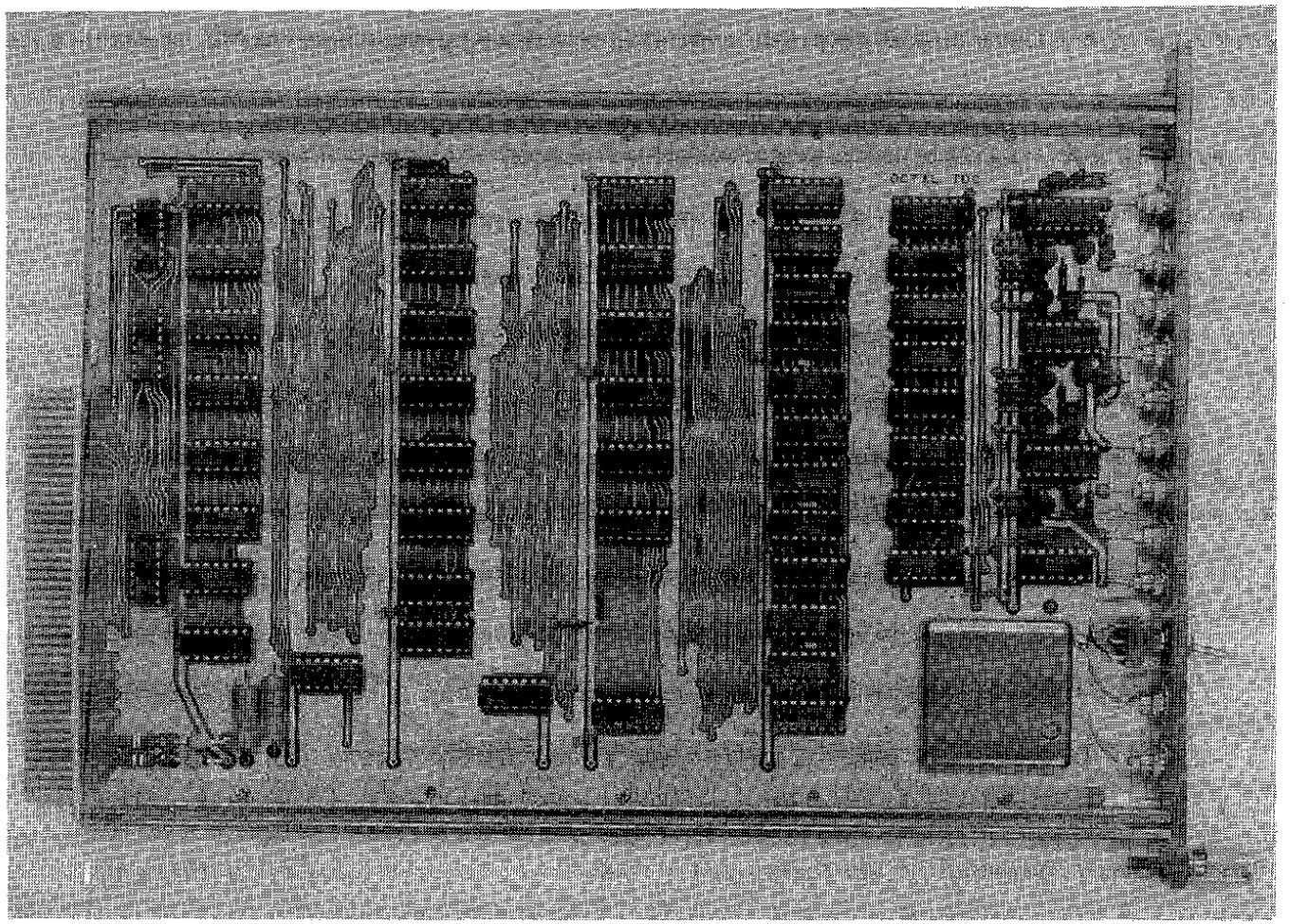
(17) POWER REQUIREMENTS:

+24V at 20mA; -24V at 50mA; +6V at 550mA; -6V at 550mA.

C11-21 OCTAL TIME TO DIGITAL CONVERTER (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C11-21)
OCTAL TIME TO DIGITAL CONVERTER KEK TYPE-1



(INSIDE VIEW)
OCTAL TIME TO DIGITAL CONVERTER KEK TYPE-1 (C11-21)

KEK CAMAC STANDARD MODULE (C11-21) C11-21-01
OCTAL TIME TO DIGITAL CONVERTER KEK TYPE-1

GENERAL

The Octal Time to Digital Converter (KEK type-1) has eight independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each channel of this module disregards any stop pulses received before a start signal and will accept only one stop for every start. The start and each stop inputs accept standard NIM fast logic signals. In the case of the internal clock mode, this module converts the measured time intervals into a 16-bit digital number at the rate of 50 MHz, for a full scale digitizing time of 1310 microseconds.

SPECIFICATIONS

(1) Common Start Input : One, common to all channels. 50 ohms impedance direct-coupled. Input amplitude > -600 mV, Lemo-type connector.

(2) Stop Inputs : Eight, one per channel. 50 ohms impedance direct-coupled. Input amplitude > -600 mV. Ineffective unless preceded by a "Start" input.

(3) Clear Input : One, common to all channels. 50 ohms impedance direct-coupled. -600 mV or greater clears. Minimum pulse width is 10 ns.

(4) Full Scale Time Range : 16-bit binary output. Giving the internal and external as two switch-selectable clock modes.
Internal clock mode, at the rate of 50 MHz, a full scale digitizing time of 1310 microseconds. External clock mode, at the maximum rate of 100 MHz, a full scale digitizing time of 655 microseconds.

(5) Data : The proper CAMAC function and addresss command gates the 16 binary bits of the selected channel onto the R(1) to R(16) Dataway bus lines.

(6) CAMAC Function Codes :

F(0)A(0-7) : Read register, requires N and A.
A(0) through A(7) are used for channel address.
F(9)A(0)S2 : Clear all registers, requires N and A(0), and S2.

(7) CAMAC Commands :

Z or C : All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2".

I : "Start" input is inhibited during CAMAC "Inhibit" command.

Q : A Q=1 response is generated in recognition of an F(0) Read function.

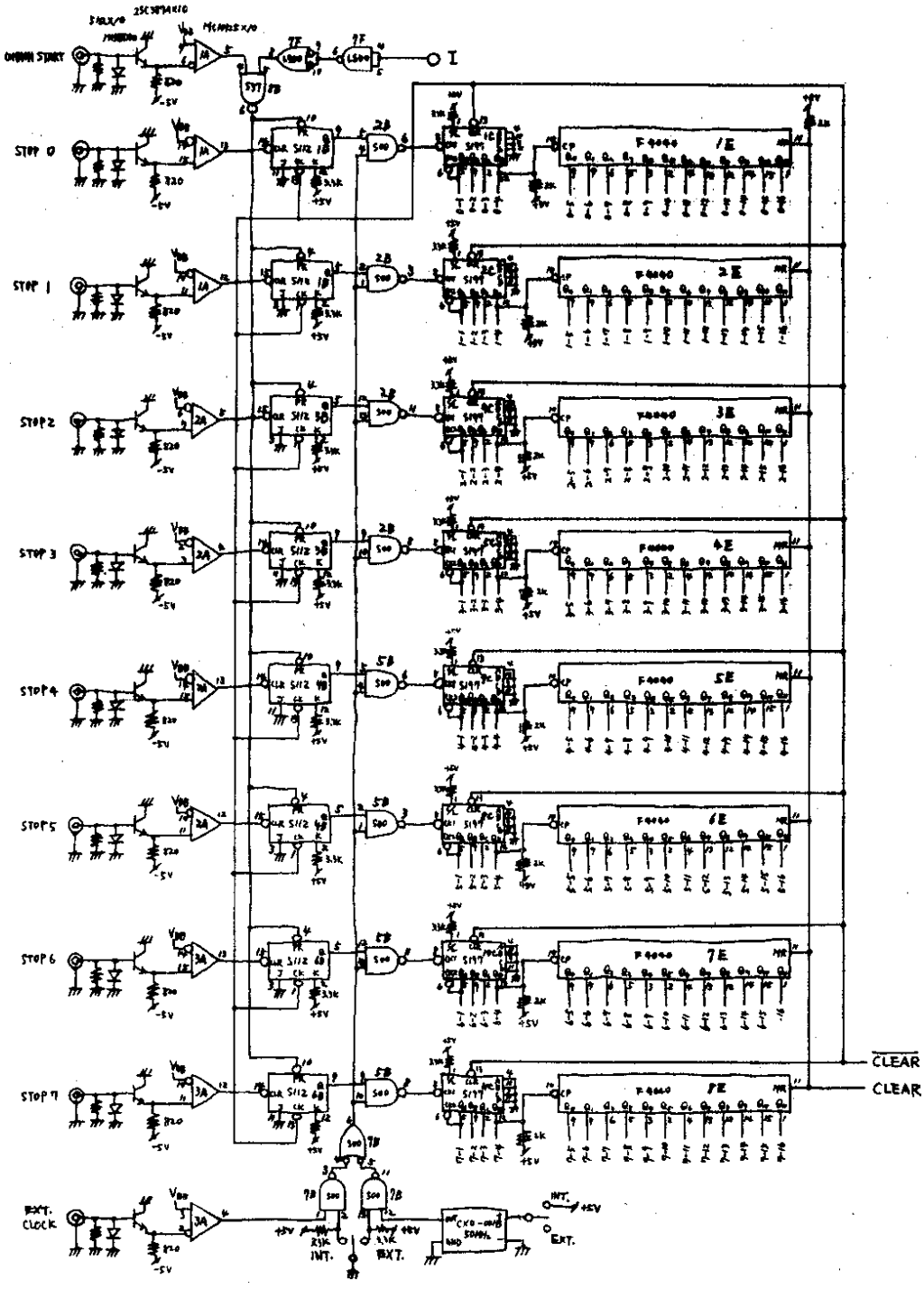
X : An X=1 (Command Accepted) response is generated when a valid F, N and A command is generated.

(8) Packaging

In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR 4100e). RF shielded CAMAC single width module.

(9) Current requirements

+6 Volts : 980 mA.
-6 Volts : 152 mA.



OCTAL TDC (I)
(C11-21)

KEK CAMAC STANDARD MODULE (C12-11) C12-11-01
10MHz CLOCK PULSE GENERATOR KEK TYPE-1

GENERAL

This module is a single width CAMAC module which contains a crystal controlled 10MHz oscillator and seven decade-divider circuits in cascade.

Thus pulses of 100ns, 1μs, 10μs, 100μs, 1ms, 10ms and 1s intervals are available at frout panel Lemo connectors at the same time.

SPECIFICATIONS

(1) Input

Impedance : 50 ohms (direct-coupled).
Voltage : "NIM" fast logic level.
Threshold level -400mV.
Width : Shortest pulse to produce full outputs <5ns (at input pulse height -600mV).
Maximum Rate : Maximum clock rate to produce full outputs >30MHz (at input pulse width 5ns).

(2) Outputs

Outputs : Eight outputs (independent output).
Quiescently 0mA, current source switches to -16mA (-800mV into 50 ohms load) during output.
Width : 36ns fixed.
Rise and Fall Time : Rise time <1.2ns.
Fall time <1.4ns.

(3) INT.OSC/EXT.OSC selection switch

Two-position front panel mounted toggle switch which selects either the internal 10MHz crystal oscillator, or the external input.

(4) Functions

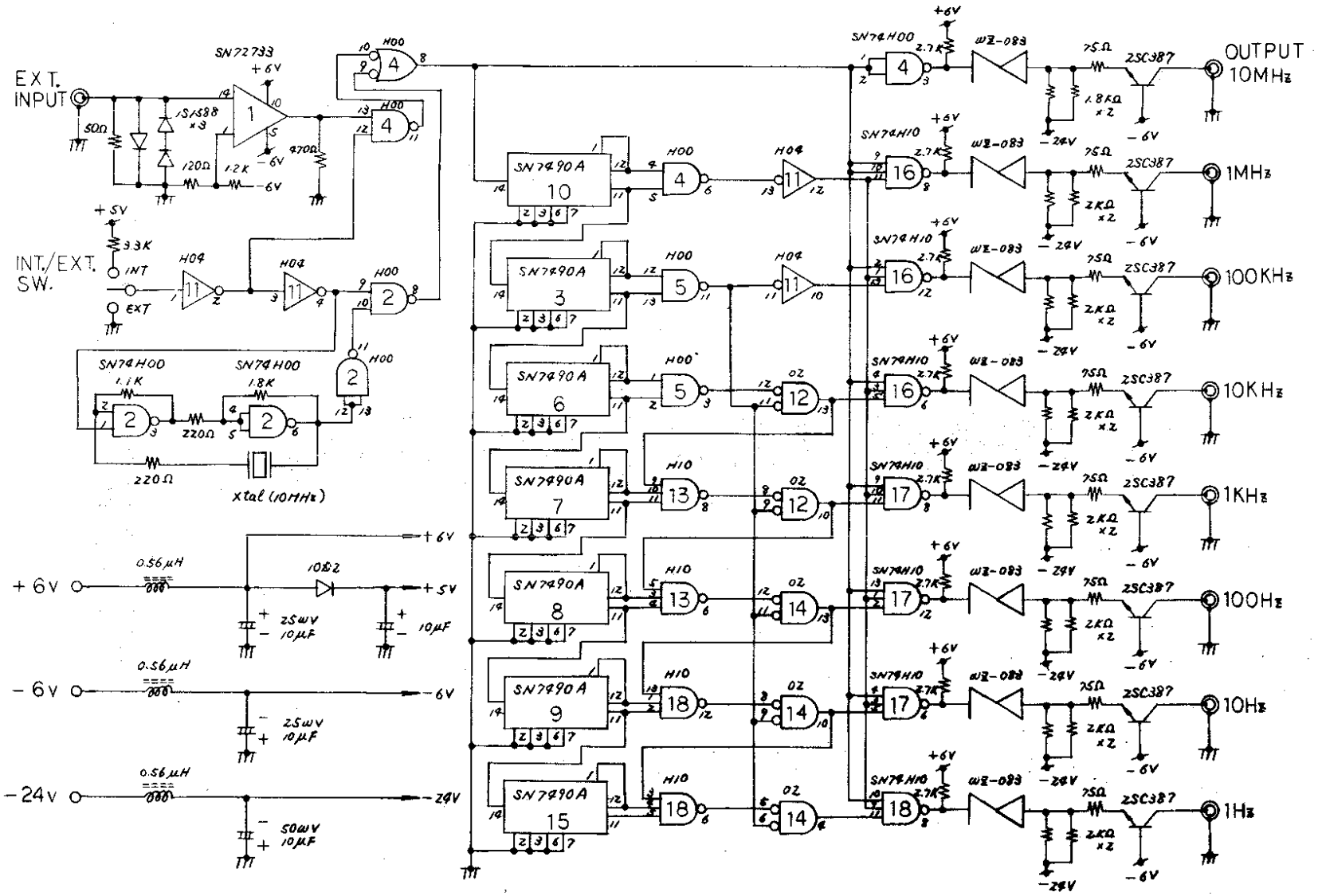
This module does not use CAMAC dataway lines other than for power lines.

(5) Power requirements

+6 Volts : 500mA.
-6 Volts : 18mA.
-24 Volts : 150mA.

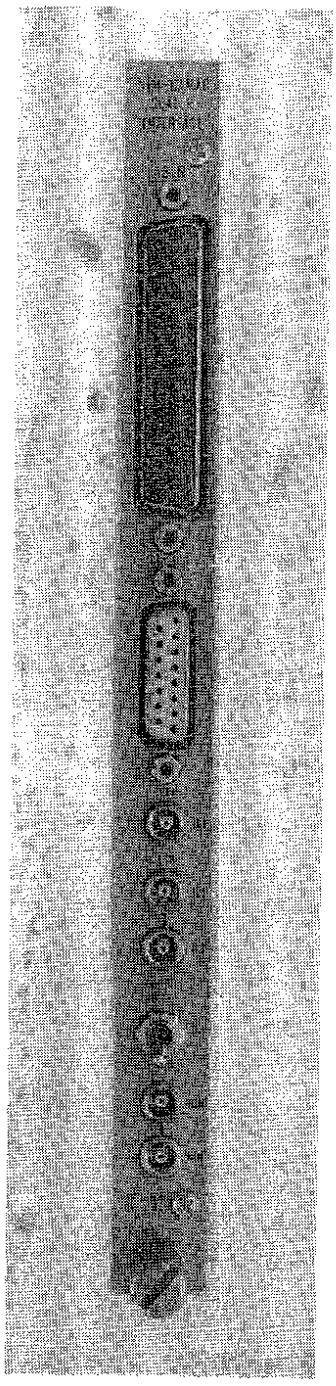
(6) Mechanical

Single width CAMAC standard module.

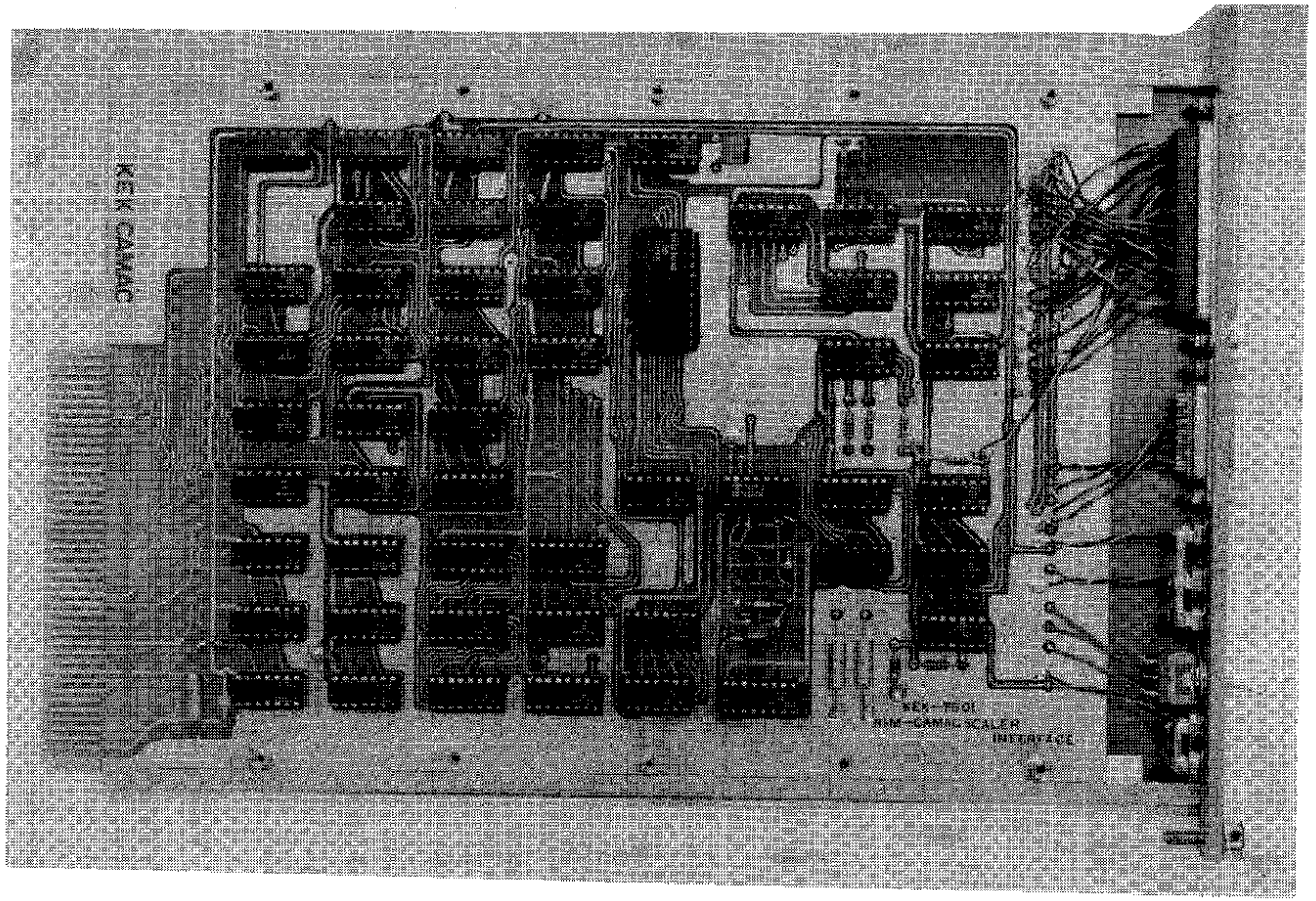


CAMAC 10MHz CLOCK PULSE GENERATOR (C12-11 KEK TYPE-1)

C13-11 NIM-CAMAC SCALER INTERFACE (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C13-11)
NIM-CAMAC SCALER INTERFACE KEK TYPE-1



(INSIDE VIEW)
NIM-CAMAC SCALER INTERFACE KEK TYPE-1 (C13-11)

KEK CAMAC STANDARD MODULE (C13-11) C13-11-01
NIM-CAMAC SCALER INTERFACE KEK TYPE-1

GENERAL

The NIM-CAMAC Scaler Interface module has been designed to control the NIM 80 MHz visual scalers (N12-22, N12-61) through the CAMAC dataway, such as start, stop, reset, data transfer, and LAM handling. One unit of this module is able to interface up to 12 the NIM visual scalers in a NIM Bin in cooperation with a Preset Scaler Controller (N12-31). The 6-digits BCD data in a NIM scaler module is read out sequentially by the data set command F(26)A(1∿12) and stored into 24-bit buffer register which is then read by the CAMAC read command F(0).

SPECIFICATIONS

(1) CAMAC functions

F(0) : Read the 24-bit data register, Produce Q response. The register should be read after the data set command F(26) A(1∿12).
F(8)A(1∿12) : Test LAM of the carry flag in any scaler. Q response is generated if LAM is set.
F(8)A(13) : Test LAM on the preset count end flag. Q response is generated if LAM is set.
F(8)A(14) : Test LAM on the external LAM. Q response is generated if LAM is set.
F(9)A(1∿12) : Clear all scalers.
F(10)A(1∿12) : Clear LAM on the carry flag.
F(10)A(13) : Clear LAM on the preset count end flag.
F(10)A(14) : Clear LAM on the external LAM.
F(24)A(13) : Disable the Start Ready gate.
F(24)A(14) : Disable the Forced Stop gate.
F(26)A(1∿12) : Set the scaler address. The NIM visual scalers are addressed with the subaddress A(1) through A(12) from the left to right in a NIM Bin.
F(26)A(13) : Enable the Start Ready gate.
F(26)A(14) : Enable the Forced Stop gate.
F(27)A(1∿12) : Test the carry flag. Produce Q response.
Z, C : Clear the 24-bit data register, the LAM register, and all the NIM scalers.
I : Inhibit counting in the NIM visual scalers except the Preset Scaler Controller.
Q : Q response is generated for F(0), F(8) and F(27).
LAM : Three bits of the LAM register are set due to the preset count end flag, the carry out signal and the external LAM signal, respectively.

(2) Front panel connectors

"BIN" : 50-pin connector. DD-50S (JAE), this is connected to the rear connector of a NIM Bin by 25 paired cable.
"CONTROL" : 15-pin connector. DA-15S (JAE), this is connected to the front panel connector of the Preset Scaler Controller by 8 paired cable.
"LAM" : External LAM signal input. TTL logic level. The external LAM bit is set at the time of the transition from high to low level.
"S.S.G." : Start Stop Gate input. TTL logic level. This gate signal is logically OR'ed with the "S.S.G."(Start Stop Gate) in the NIM Bin. The low level corresponds to the open gate.
"INHIBIT" : External inhibit signal input. NIM logic level. Input impedance is 1 Kohms. This signal inhibits all scalers to count except the Preset Scaler Controller.
Toggle switch : "BOTH", the scalers are inhibited by both signals of internal CAMAC dataway I and external inhibit signal above.
"FRONT", only the inhibit signal from the front panel is effective.

(3) Power requirement

+6 Volts : 860 mA.
-6 Volts : 20 mA.

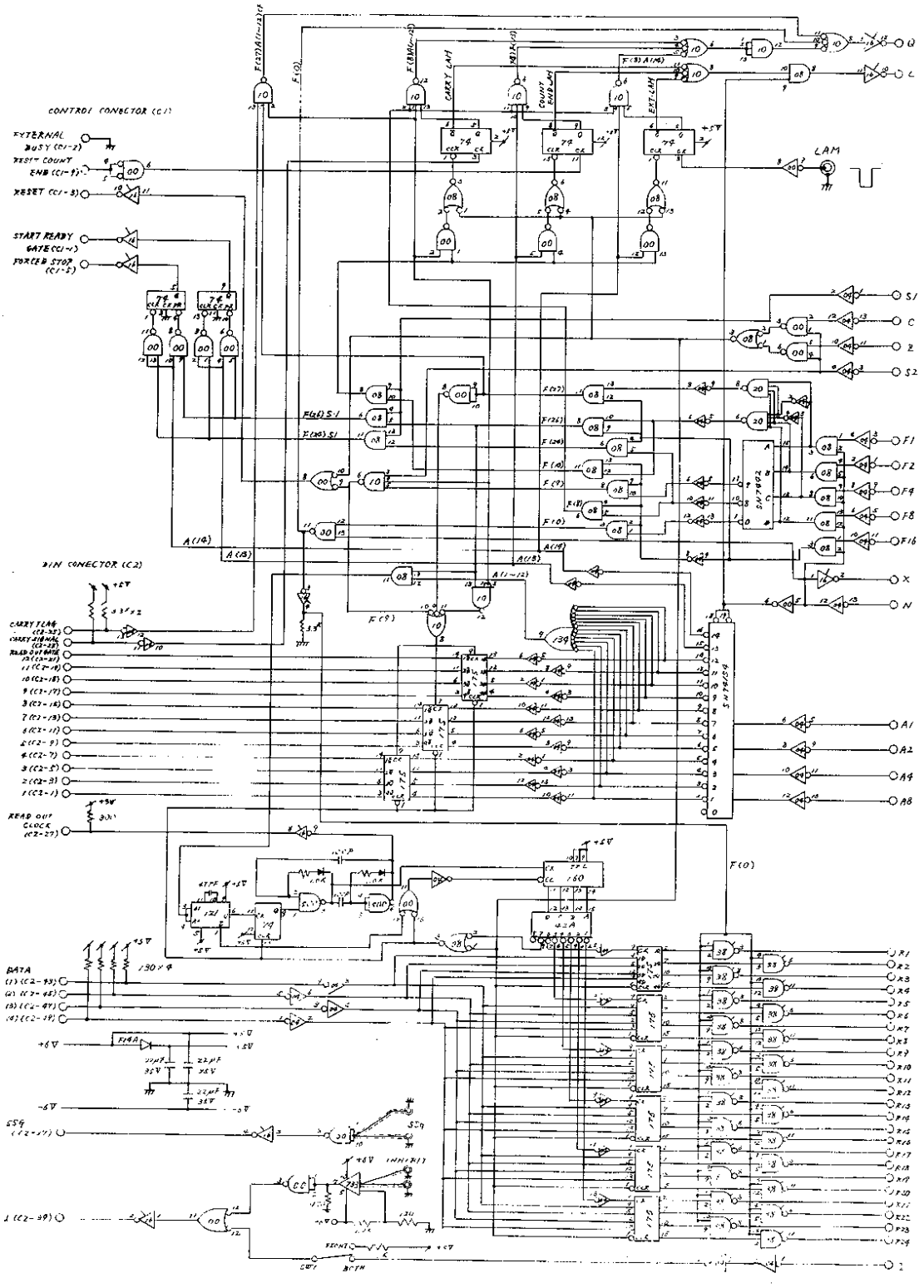
(4) Mechanical

Single width CAMAC standard module.

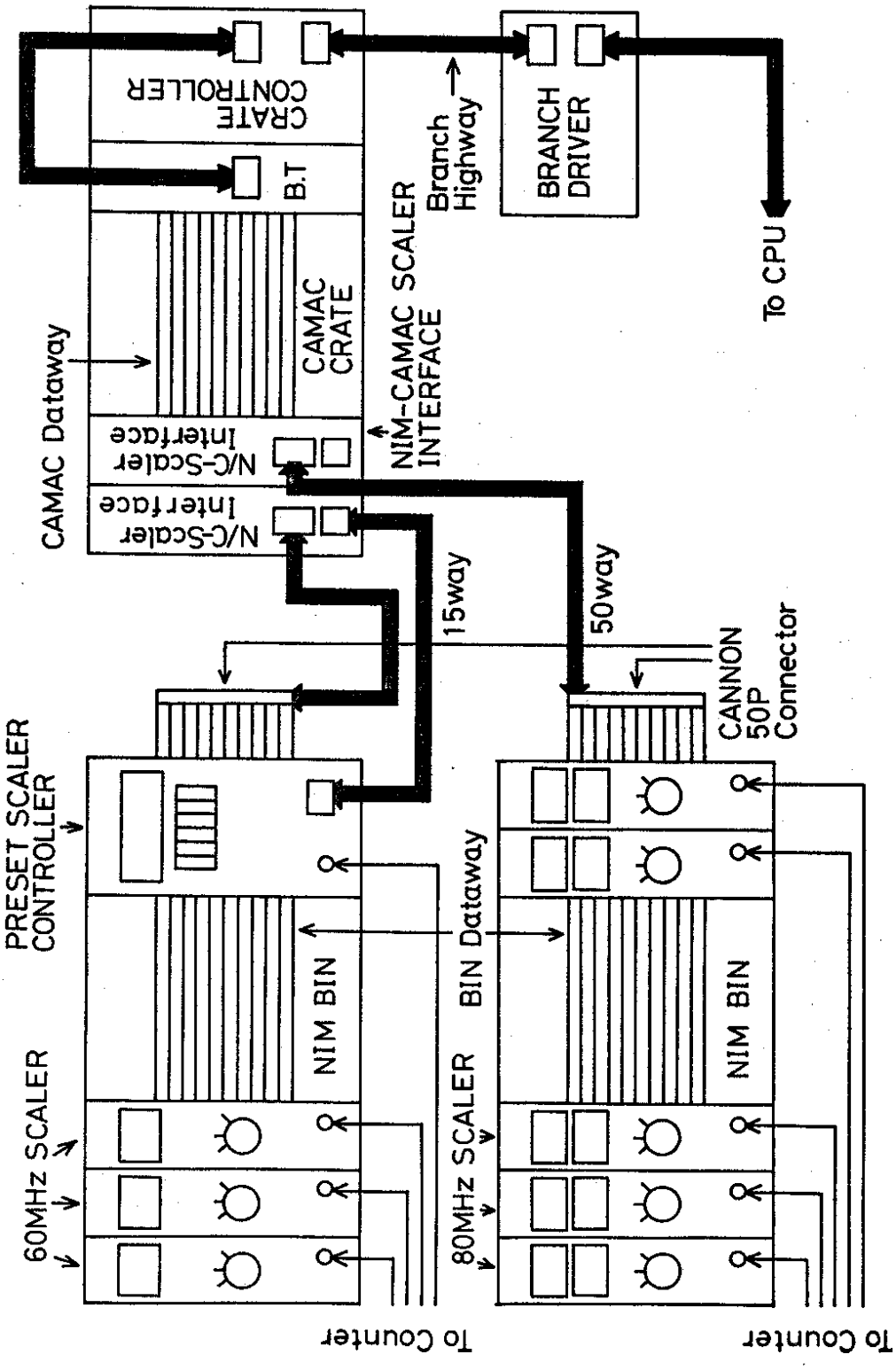
(5) Software note

The data read-out sequence is described below for PDP 11/45.

```
---
MOV   #3221, @#166010; F(26)N(1)A(1) DATA SET
TST   @#166000
BPL   .-4
MOV   #20, @#166010; F(0)N(1)A(0) READ REGISTER
TST   @#166000
BPL   .-4
MOV   @#166002, R0; TRANSFER DATA TO R0
---
```



NIM-CAMAC SCALER INTERFACE KEK TYPE-I (C13-11)



Functional diagram of the scaler system

PIN	FUNCTION
1	START READY GATE
2	EXTERNAL BUSY
3	RESET SIGNAL
4	RESET SIGNAL PAIR RETURN
5	FORCED STOP SIGNAL
6	FORCED STOP SIGNAL PAIR RETURN
7	START READY
8	START READY PAIR RETURN
9	PRESET COUNT END FLAG
10	ON-LINE FLAG
11	START STOP GATE
12	START STOP GATE PAIR RETURN
13	START SIGNAL
14	STOP SIGNAL
15	POWER RETURN GND

USED CONNECTOR DA-15S-ZN

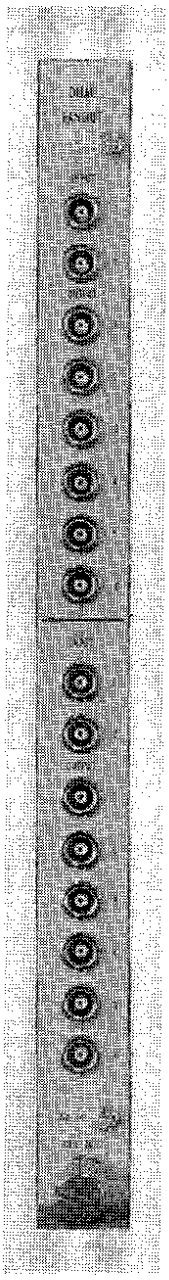
PRESET SCALER CONTROLLER
EXTERNAL CONTROL CONNECTOR
PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	READ-OUT GATE 1	31	
2	PIN 1 PAIR RETURN	32	
3	READ-OUT GATE 2	33	PIN 17 PAIR RETURN
4	PIN 3 PAIR RETURN	34	PIN 18 PAIR RETURN
5	READ-OUT GATE 3	35	RESET
6	PIN 5 PAIR RETURN	36	PIN 35 PAIR RETURN
7	READ-OUT GATE 4	37	START STOP GATE
8	PIN 7 PAIR RETURN	38	PIN 37 PAIR RETURN
9	READ-OUT GATE 5	39	INHIBIT
10	PIN 9 PAIR RETURN	40	PIN 39 PAIR RETURN
11	READ-OUT GATE 6	41	BEAM GATE
12	PIN 11 PAIR RETURN	42	PIN 41 PAIR RETURN
13	READ-OUT GATE 7	43	DATA (1)
14	PIN 13 PAIR RETURN	44	PIN 43 PAIR RETURN
15	READ-OUT GATE 8	45	DATA (2)
16	PIN 15 PAIR RETURN	46	PIN 45 PAIR RETURN
17	READ-OUT GATE 9	47	DATA (4)
18	READ-OUT GATE 10	48	PIN 47 PAIR RETURN
19	READ-OUT GATE 11	49	DATA (8)
20	PIN 19 PAIR RETURN	50	PIN 49 PAIR RETURN
21	READ-OUT GATE 12		
22	PIN 21 PAIR RETURN		
23	CARRY SIGNAL		
24	PIN 23 PAIR RETURN		
25	CARRY FLAG		
26	PIN 25 PAIR RETURN		
27	READ-OUT CLOCK		
28	PIN 27 PAIR RETURN		
29	SKIP		
30	PIN 29 PAIR RETURN		

NIM BIN KEK TYPE-2
CONTROL (Dataway) CONNECTOR
PIN ASSIGNMENTS

USED CONNECTOR: DDC-50S-FO
(Cannon)

C14-11 DUAL FANOUT (KEK TYPE-1)



KEK CAMAC STANDARD MODULE (C14-11)
DUAL FANOUT KEK TYPE-1

KEK CAMAC STANDARD MODULE (C14-11)
DUAL FAN OUT KEK TYPE-1

SPECIFICATIONS

(1) INPUT

Number of Channels: Two

Inputs: 2 per channel
Direct-coupled

Impedance: 50ohms

Voltage: Threshold according to "NIM" specifications
Threshold level -500mV

Width: Shortest pulse to produce full output
< 3ns for logic input (at -600mV)

Maximum Rate: Maximum repetition rate to produce full output
> 140 MHZ

(2) OUTPUT

Outputs: For every single input, 6 normal outputs

Voltage: When output is loaded with 50ohms
-800mV (independent each output)

Rise and Fall Time: Rise time < 800ps
Fall time < 800ps

Overshoot: < 15%

Undershoot: < 4%

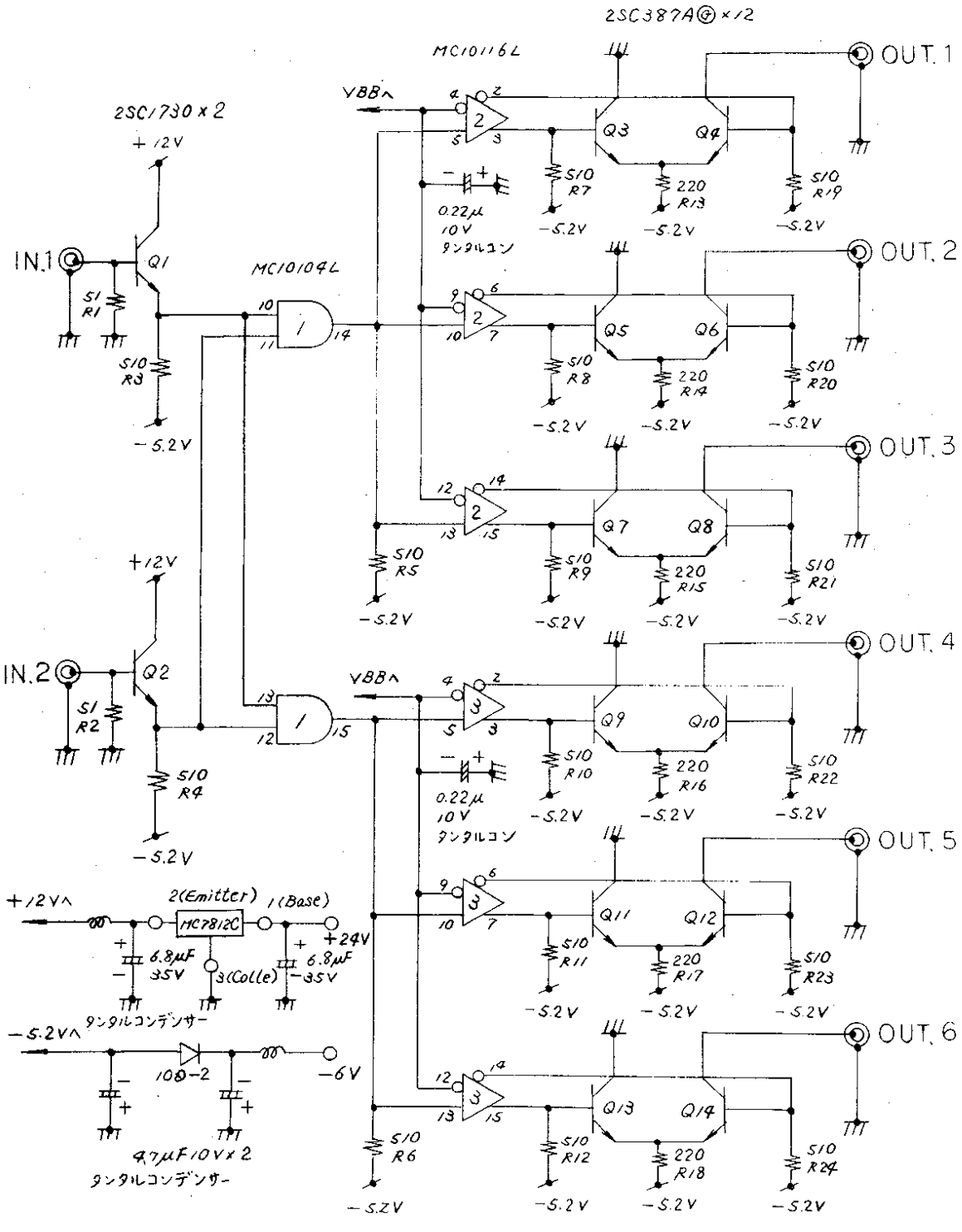
Propagation Delay Time: 7ns

(3) POWER CONSUMPTION

+24 Volts: 37mA

-6 Volts: 525mA

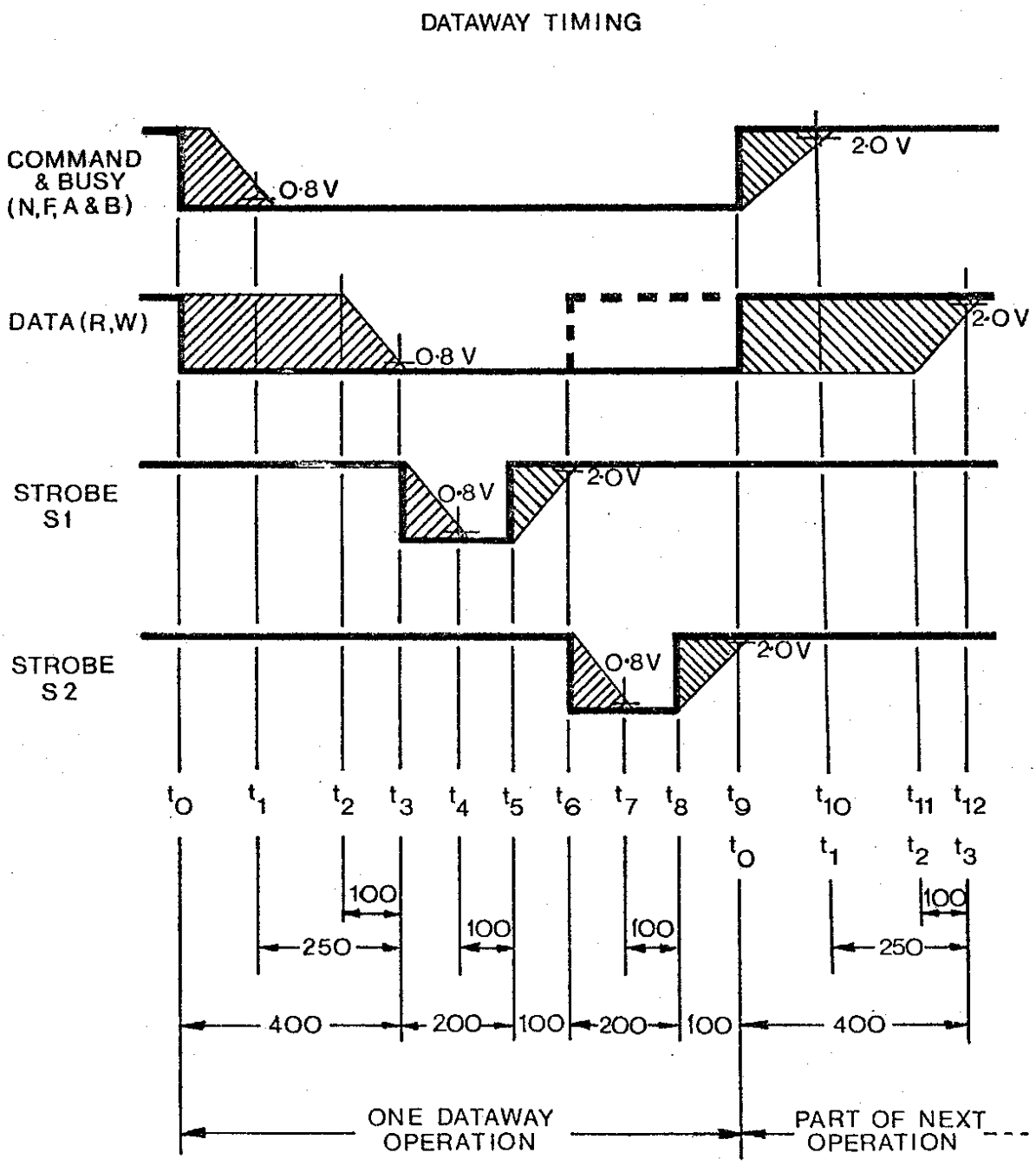
(4) DIMENSION: "CAMAC" standard single width module



CAMAC DUAL FANOUT (C14-11 KEK TYPE-1)

APPENDIX 1
Command Timing Diagram of the CAMAC Dataway

CAMAC
COMMAND TIMING
DIAGRAM



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

APPENDIX 2
Listing CAMAC Dataway Pin Usage

STANDARD DATAWAY USAGE

TITLE	DISIGNATION	CONTACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module(Individual line from control station).
Sub-Address	A1,2,4,8	4	Selects a section of the module.
Function	F1,2,4,8,16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation(Dataway signals must not change).
Strobe 2	S2	1	Controls second phase(Dataway signals may change).
Data			
Write	W1-W24	24	Bring information to the modul.
Read	R1-R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service(Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			
Initialise	Z	1	Operate on all features connected to them, no command required.
Inhibit	I	1	Sets module to a defined state.(Accompanied by S2 and B).
Clear	C	1	Disables features for duration of signal. Clears registers.(Accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1,P2	2	For unspecified uses.
Patch contacts	P3-P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			The crate is wired for mandatory and additional lines.
+24V d.c.	+24	1	
+6V d.c.	+6	1	
-6V d.c.	-6	1	
-24V d.c.	-24	1	
0V	0	2	Power return.
Additional Power Lines			
+200V d.c.	+200	1	Lines are reserved for the following power supplies
+12V d.c.	+12	1	Low current for indicators etc.
-12V d.c.	-12	1	
117V a.c.(Live)	ACL	1	
117V a.c.(Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved	Y1,Y2	2	Reserved for future allocation.
TOTAL		86	

APPENDIX 3
Pin Allocation at Normal Station of the CAMAC Dataway

Pin Allocation at Normal Station Viewed from Front of Crate

Individual Patch Point		P1	B	Busy	Bus Line
" " "		P2	F16	Function	" "
" " "		P3	F8	"	" "
" " "		P4	F4	"	" "
" " "		P5	F2	"	" "
Bus Line	- Reserved	X	F1	"	" "
" " with patch point	- Inhibit	I	A8	Sub-Address	" "
" " " " "	- Clear	C	A4	"	" "
Individual Lines	- Station No.	N	A2	"	" "
with patch points	- Look-at-Me	L	A1	"	" "
Bus Line	- Strobe 1	S1	Z	Initialise	" "
Bus Line	- Strobe 2	S2	Q	Response	" "
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus Lines		W16	W15		
W1 = least significant bit		W14	W13		
W24 = most significant bit		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3.		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus Lines		R16	R15		
R1 = least significant bit		R14	R13		
R24 = most significant bit		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
Reserved for -12 volts d.c.		-12	-24	-24 volts d.c.	
Reserved for +200 volts d.c.		+200	- 6	- 6 volts d.c.	
Reserved 117 volts a.c. Live		ACL	ACN	Reserved for 117 volts a.c. Neutral	
Reserved		Y1	E	Reserved for Clean Earth	
Reserved for +12 volts d.c.		+12	+24	+24 volts d.c.	
Reserved		Y2	+6	+ 6 volts d.c.	
0 volts (Power return)		0	0	0 volts (Power return)	

APPENDIX 4
Pin Allocation at Normal Station of the CAMAC Dataway

Pin Allocation at Control Station Viewed from Front of Crate

Individual Patch Point		P1	B	Busy	Bus Line
" " "		P2	F16	Function	" "
" " "		P3	F8	"	" "
" " "		P4	F4	"	" "
" " "		P5	F2	"	" "
Bus Line	- Reserved	X	F1	"	" "
" " with patch point	- Inhibit	I	A8	Sub-Address	" "
" " " " "	- Clear	C	A4	"	" "
Individual Patch Point		P6	A2	"	" "
" " "		P7	A1	"	" "
Bus Line	- Strobe 1	S1	Z	Initialise	" "
Bus Line	- Strobe 2	S2	Q	Response	" "
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 Individual Look-at-Me Lines		L13	N13	24 Individual Station Lines	
		L12	N12		
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
Reserved for -12 volts d.c.		-12	-24	-24 volts d.c.	
Reserved for +200 volts d.c.		+200	- 6	- 6 volts d.c.	
Reserved for 117 volts a.c. Live		ACL	ACN	Reserved for 117 volts a.c. Neutral	
Reserved		Y1	E	Reserved for Clean Earth	
Reserved for +12 volts d.c.		+12	+24	+24 volts d.c.	
Reserved		Y2	+ 6	+ 6 volts d.c.	
0 volts (Power return)		0	0	0 volts (Power return)	

APPENDIX 5
Function Codes with CAMAC Command

CAMAC FUNCTION CODES

R/W	CODE F( )	FUNCTION
R	0	Read Group 1 Register
R	1	Read Group 2 Register
R	2	Read and Clear Group 1 Register
R	3	Read Complement of Group 1 Register
R	4	Non-standard
R	5	Reserved
R	6	Non-standard
R	7	Reserved
	8	Test Look-at-Me
	9	Clear Group 1 Register
	10	Clear Look-at-Me
	11	Clear Group 2 Register
	12	Non-standard
	13	Reserved
	14	Non-standard
	15	Reserved
W	16	Overwrite Group 1 Register
W	17	Overwrite Group 2 Register
W	18	Selective Set Group 1 Register
W	19	Selective Set Group 2 Register
W	20	Non-standard
W	21	Selective Clear Group 1 Register
W	22	Non-standard
W	23	Selective Clear Group 2 Register
	24	Disable
	25	Execute
	26	Enable
	27	Test Status
	28	Non-standard
	29	Reserved
	30	Non-standard
	31	Reserved

GROUP 2 REGISTERS ADDRESS ASSIGNMENTS
A(12) LAM Source Register.
A(13) LAM Mask.
A(14) "Masked" LAM's.
A(15) Module Identifying Number.

APPENDIX 6
Signal Lines at Branch Highway Ports

Signal Lines at Branch Highway Ports

Title	Designation	Generated By	Signal Lines	Use
Command				
Crate address	BCR1 - BCR7	Branch driver	7	Each line addresses one crate in the branch
Station number	BN1,2,4,8,16	Branch driver	5	Binary coded station number
Sub-address	BA1,2,4,8	Branch driver	4	As on Dataway A lines
Function	BF1,2,4,8,16	Branch driver	5	As on Dataway F lines
Data				
Read/Write	BRW1-BRW24	Branch driver (W) or Crate controller (R)	24	For Read data, Write data and Graded-L
Response	BQ	Crate controller	1	As on Dataway Q line
Timing				
Timing A	BTA	Branch driver	1	Indicates presence of Command, etc.
Timing B	BTB1-BTB7	Crate controller	7	Each line indicates presence of data, etc., from one crate controller
Demand Handling				
Branch demand	BD	Crate controller	1	Indicates presence of demand
Graded-L request	BG	Branch driver	1	Requests Graded-L Operation
Common Controls				
Initialise	BZ	Branch driver	1	As on Dataway Z line
Spare				
Reserved	BX1 - BX9		9	For future requirements

APPENDIX 7
Contact Assignments at Branch Highway Ports, By Function

Contact Assignments at Branch Highway Ports: By Function

Twisted Pairs					Twisted Pairs		
Signal Pin	Return Pin	Signal			Signal Pin	Return Pin	Signal
93	76	BRW1			32	13	BCR1
94	77	BRW2			33	14	BCR2
95	78	BRW3			34	15	BCR3
96	79	BRW4		CRATE	35	16	BCR4
97	80	BRW5		SELECTOR	67	50	BCR5
98	81	BRW6			68	51	BCR6
99	82	BRW7			69	52	BCR7
100	83	BRW8					
103	84	BRW9			36	17	BN1
104	85	BRW10			37	18	BN2
105	86	BRW11		STATION	38	19	BN4
106	87	BRW12	READ/	ADDRESS	39	20	BN8
107	88	BRW13	WRITE		40	21	BN16
108	89	BRW14	LINES				
109	90	BRW15			41	1	BA1
110	91	BRW16		SUB-	23	2	BA2
112	113	BRW17		ADDRESS	24	3	BA4
114	115	BRW18			25	4	BA8
116	117	BRW19					
118	119	BRW20			70	53	BF1
124	125	BRW21		FUNCTION	71	54	BF2
126	127	BRW22		CODE	72	55	BF4
128	129	BRW23			73	56	BF8
130	131	BRW24			74	57	BF16
26	5	BX1		GO	63	46	BTA
27	6	BX2					
28	7	BX3			31	10	BTB1
29	8	BX4	SPARE		11	12	BTB2
30	9	BX5	PAIRS	REPLY	58	22	BTB3
64	47	BX6		LINES	132	92	BTB4
65	48	BX7			123	102	BTB5
66	49	BX8			120	101	BTB6
111	75	BX9			121	122	BTB7
59	42	BG	GRANT	RESPONSE	61	44	BQ
60	43	BD	DEMAND	INITIALISE	62	45	BZ

APPENDIX 8
Contact Assignments at Branch Highway Ports, By Contact Number

Contact Assignments at Branch Highway Ports: By Contact Number

Contact Line		Contact Line		Contact Line		Contact Line		Contact Line		Contact Line		Contact Line		Contact Line	
1	BA1(R)	18	BN2(R)	35	BCR4	52	BCR7(R)	69	BCR7	86	BRW11(R)	103	BRW9	120	BTB6
2	BA2(R)	19	BN4(R)	36	BN1	53	BF1(R)	70	BF1	87	BRW12(R)	104	BRW10	121	BTB7
3	BA4(R)	20	BN8(R)	37	BN2	54	BF2(R)	71	BF2	88	BRW13(R)	105	BRW11	122	BTB7(R)
4	BA8(R)	21	BN16(R)	38	BN4	55	BF4(R)	72	BF4	89	BRW14(R)	106	BRW12	123	BTB5
5	BX1(R)	22	BTB3(R)	39	BN8	56	BF8(R)	73	BF8	90	BRW15(R)	107	BRW13	124	BRW21
6	BX2(R)	23	BA2	40	BN16	57	BF16(R)	74	BF16	91	BRW16(R)	108	BRW14	125	BRW21(R)
7	BX3(R)	24	BA4	41	BA1	58	BTB3	75	BX9(R)	92	BTB4(R)	109	BRW15	126	BRW22
8	BX4(R)	25	BA8	42	BG(R)	59	BG	76	BRW1(R)	93	BRW1	110	BRW16	127	BRW22(R)
9	BX5(R)	26	BX1	43	BD(R)	60	BD	77	BRW2(R)	94	BRW2	111	BX9	128	BRW23
10	BTB1(R)	27	BX2	44	BQ(R)	61	BQ	78	BRW3(R)	95	BRW3	112	BRW17	129	BRW23(R)
11	BTB2	28	BX3	45	BZ(R)	62	BZ	79	BRW4(R)	96	BRW4	113	BRW17(R)	130	BRW24
12	BTB2(R)	29	BX4	46	BTA(R)	63	BTA	80	BRW5(R)	97	BRW5	114	BRW18	131	BRW24(R)
13	BCR1(R)	30	BX5	47	BX6(R)	64	BX6	81	BRW6(R)	98	BRW6	115	BRW18(R)	132	BTB4
14	BCR2(R)	31	BTB1	48	BX7(R)	65	BX7	82	BRW7(R)	99	BRW7	116	BRW19		
15	BCR3(R)	32	BCR1	49	BX8(R)	66	BX8	83	BRW8(R)	100	BRW8	117	BRW19(R)		
16	BCR4(R)	33	BCR2	50	BCR5(R)	67	BCR5	84	BRW9(R)	101	BTB6(R)	118	BRW20		
17	BN1(R)	34	BCR3	51	BCR6(R)	68	BCR6	85	BRW10(R)	102	BTB5(R)	119	BRW20(R)		

NOTE:- BRW1(R) is the return line corresponding to BRW1.

APPENDIX 9
Contact Assignments for Rear Connector of Crate Controller

Contact Assignment for Rear Connector of Crate Controller

Contact	Usage	Contact	Usage
1	Graded-L Operation	2	L1
3	GL1	4	L2
5	GL2	6	L3
7	GL3	8	L4
9	GL4	10	L5
11	GL5	12	L6
13	GL6	14	L7
15	GL7	16	L8
17	GL8	18	L9
19	GL9	20	L10
21	GL10	22	L11
23	GL11	24	L12
25	GL12	26	L13
27	GL13	28	L14
29	GL14	30	L15
31	GL15	32	L16
33	GL16	34	L17
35	GL17	36	L18
37	GL18	38	L19
39	GL19	40	L20
41	GL20	42	L21
43	GL21	44	L22
45	GL22	46	L23
47	GL23	48	External D.
49	GL24	50	N(28)+N(30) *
51	Ext. Inhibit	52	OV.

* Controller Addressed